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A Low-Cost Teaching & Research Platform Based on Xilinx RFSoC Technology and the PYNQ Framework

INTERNATIONAL SYMPOSIUM ON FIELD-PROGRAMMABLE GATE ARRAYS TUTORIAL

28th February 2021

RFSoC 2x2 Demonstrations & Edu Support & SDR Design Notebooks

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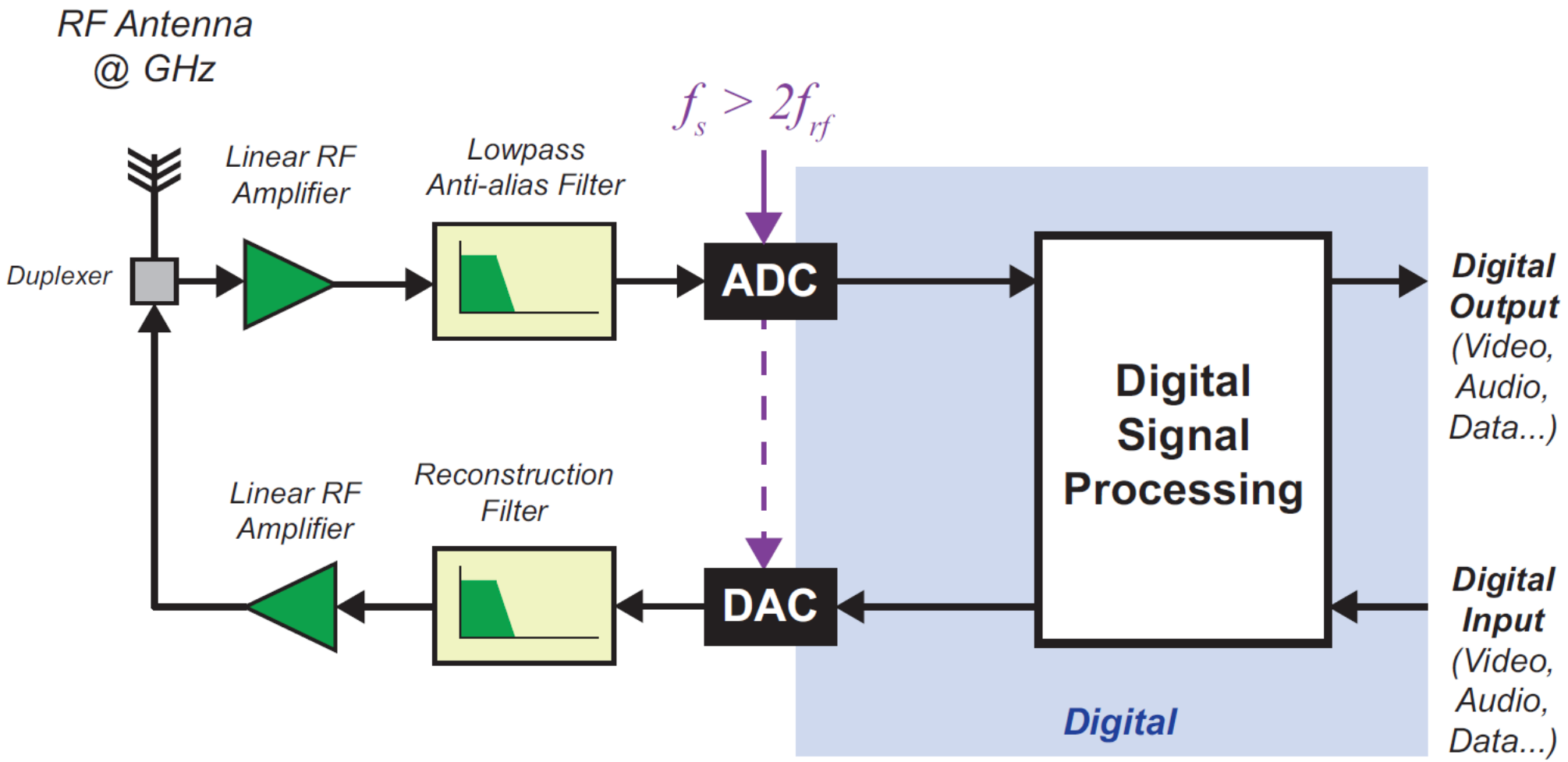
University of Strathclyde, XUP Partner

Software Defined Radio with the RFSoC (‘*GHz Sampling*’)



(A DSP Engineers wishful thinking from 1997…)

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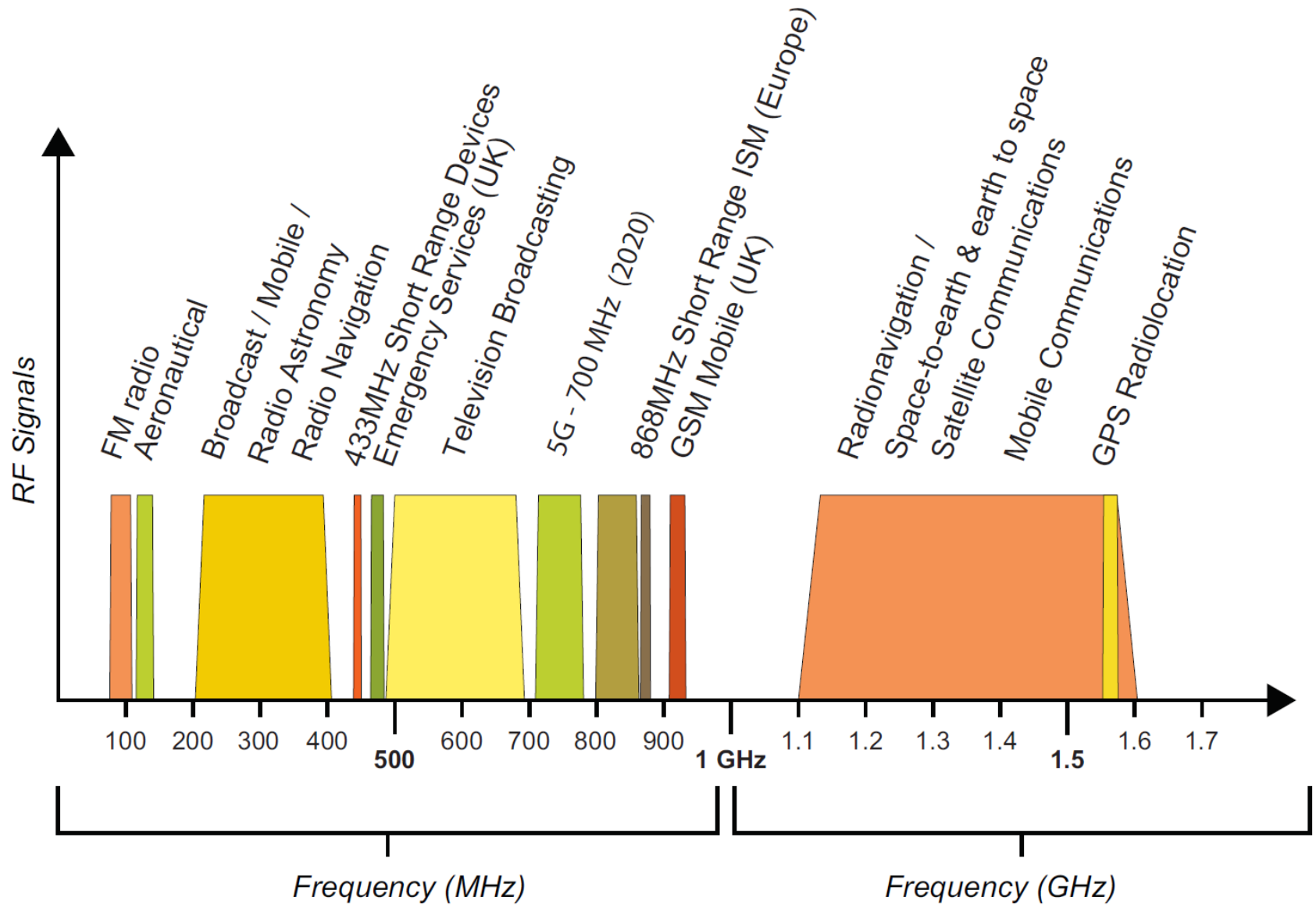
RFSoC 2x2 – Scanning the RF Spectrum

In this section we will run **live** on the RFSoC 2x2:

- The **Spectrum Analyser** comes on the base overlay – ready to run!
- We first set up the RFSoC 2x2 with just a **low cost wideband antenna ($2)**
- Next we will 'live' scan/view the **RF spectrum from 90 MHz to 4 GHz**
- We can identify some **spectral characteristics** and identify signal types
- We will add a single stage of low pass **anti-alias filtering** front end stages
- Next we show how add in simple **wideband low noise** amplifier stage
- And use of the **frequency planner** will be demonstrated
- We can **receive signals** in the 2nd Order Nyquist zone (WiFi example)

Some of the RF Spectrum (UK): 100 MHz to 1.7 GHz



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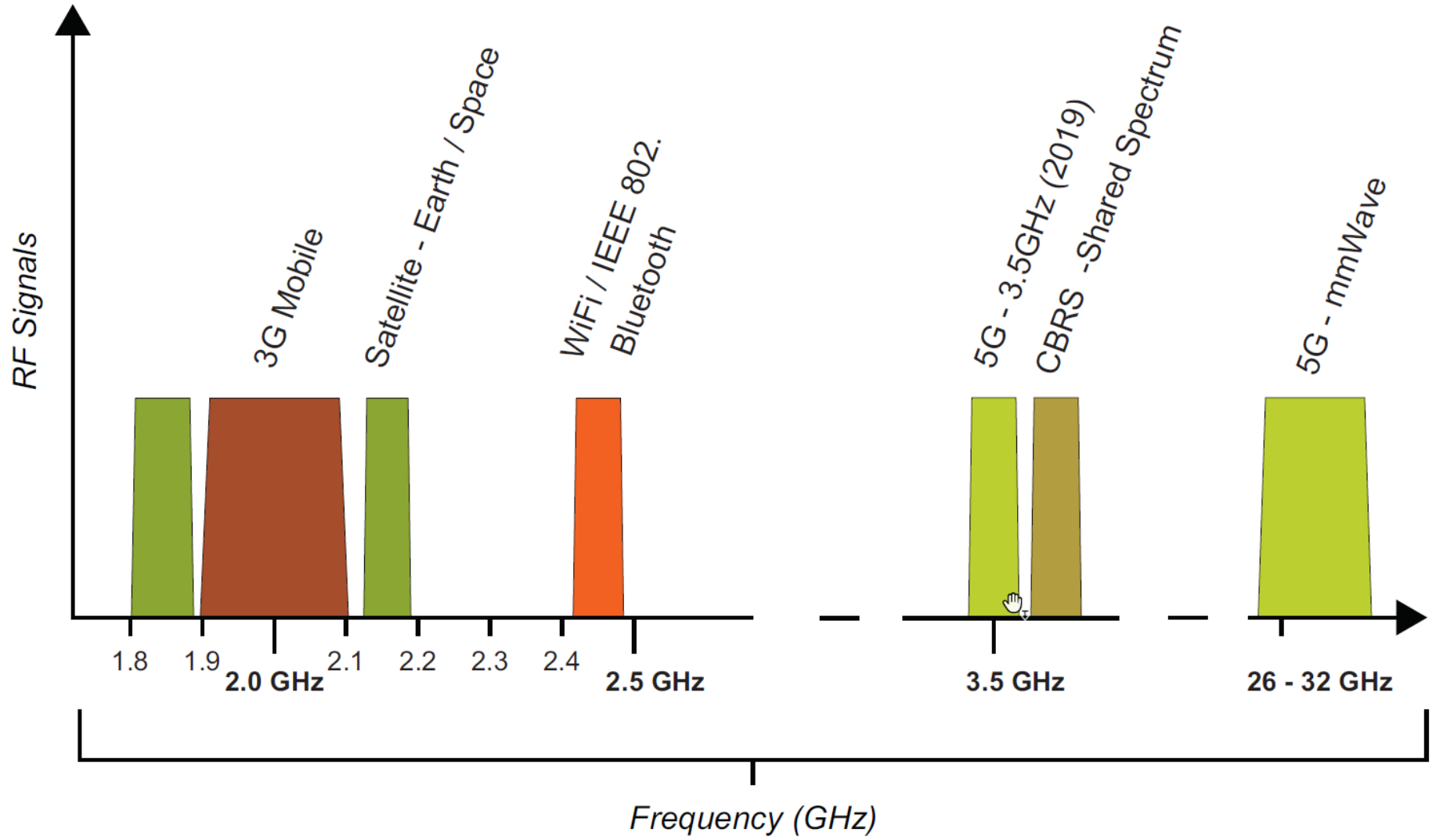
Some of the RF Spectrum (UK): 1.8 GHz to 32 GHz



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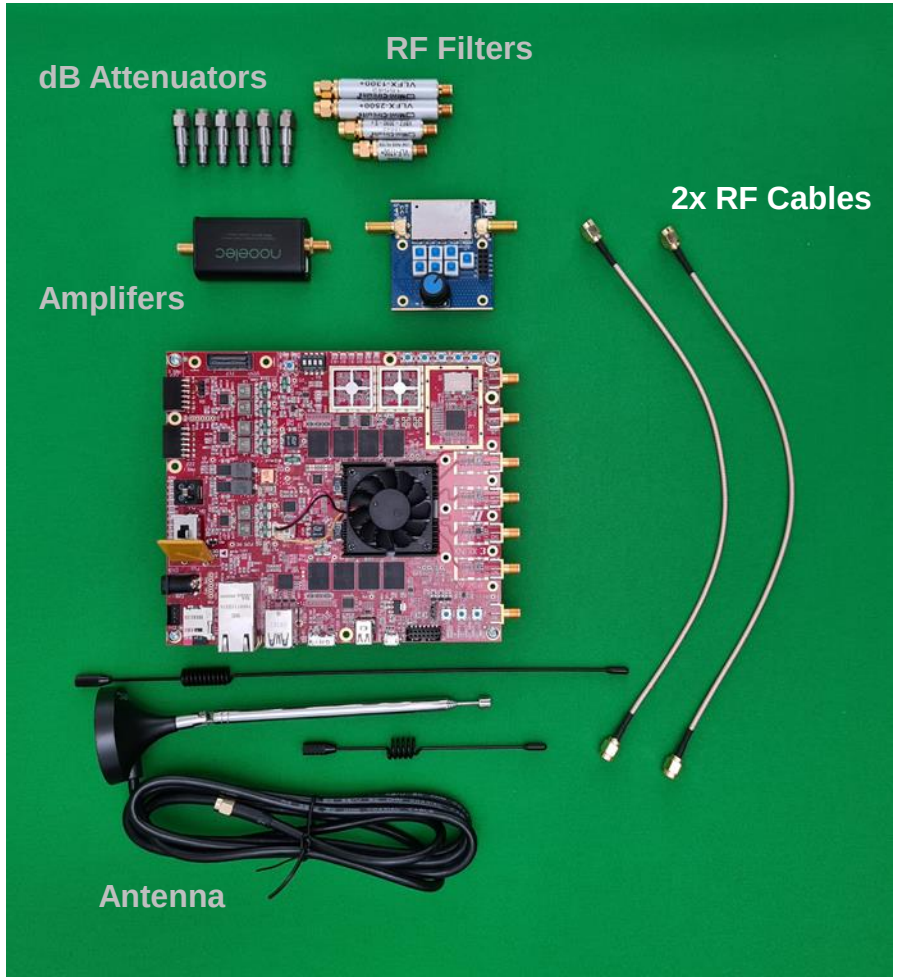
Open the Box and Getting Started (…fast!)

In the Box …

- RFSoC 2x2 + cables + power supply
- SMA cable for loopback test (RF DAC to RF ADC)

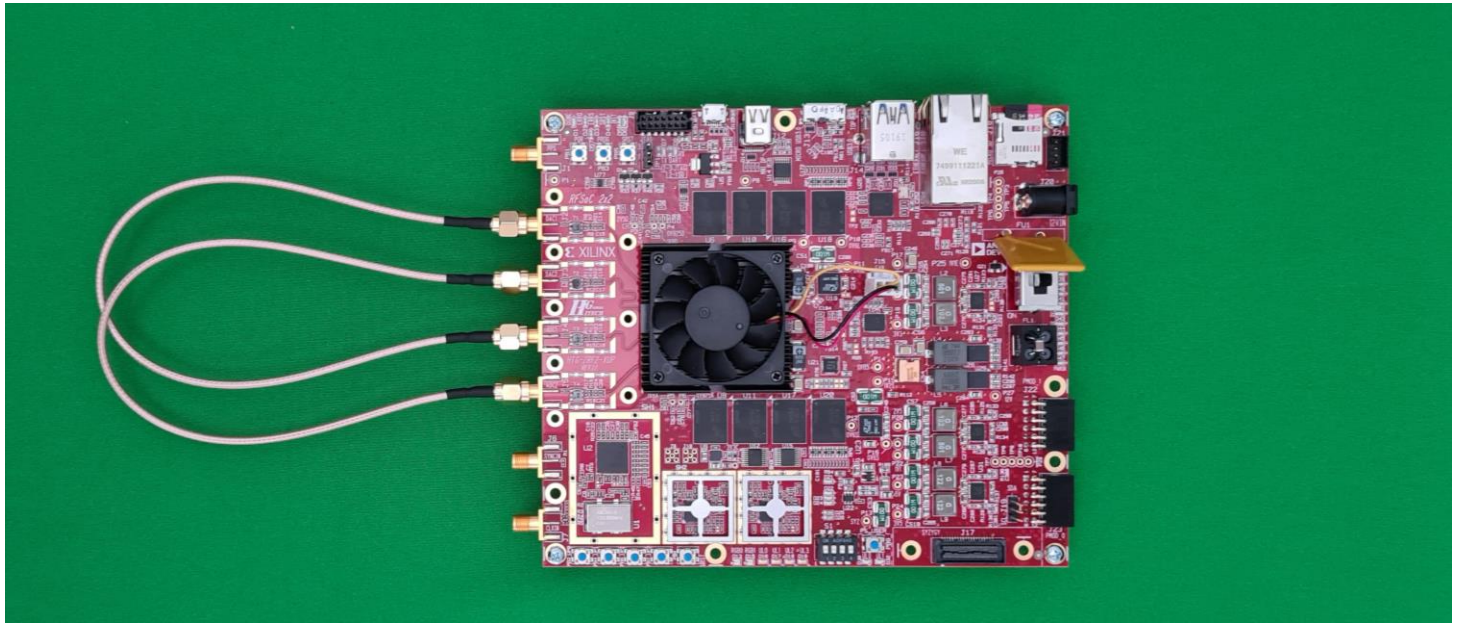
Useful Low Cost Add-ons for RF Receiving:

- Simple wideband SMA connector antenna(s)
- Wideband low noise ampifiers
- Selection of SMA in-line filters
- Selection of SMA in line dB attenuators

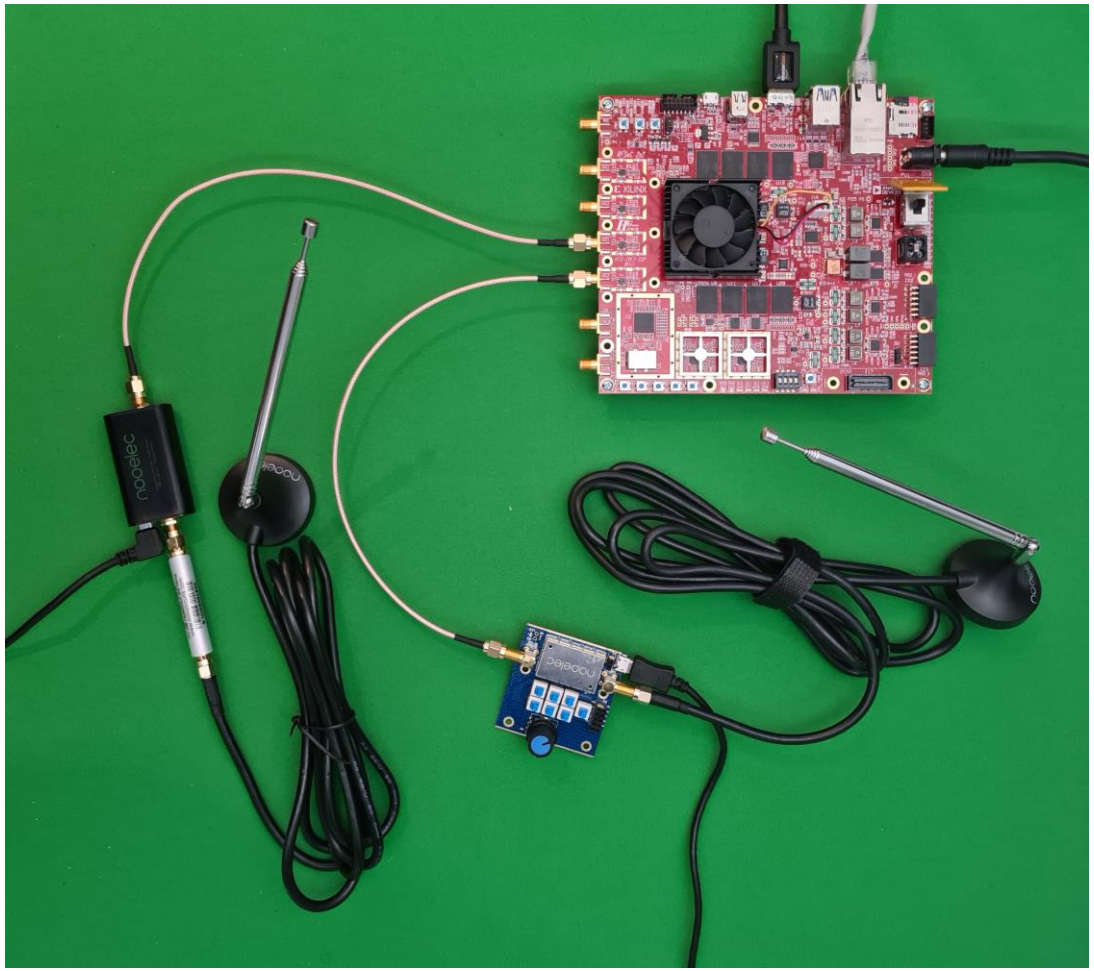


Loopback – Instant RF Signal Tx and Rx Setup

- Connect output of RF DAC-0 to input of RF ADC-0
- Connect output of RF DAC-1 to input of RF ADC-1



A Few Components More … 2x Amplifiers, 2 x Antennas



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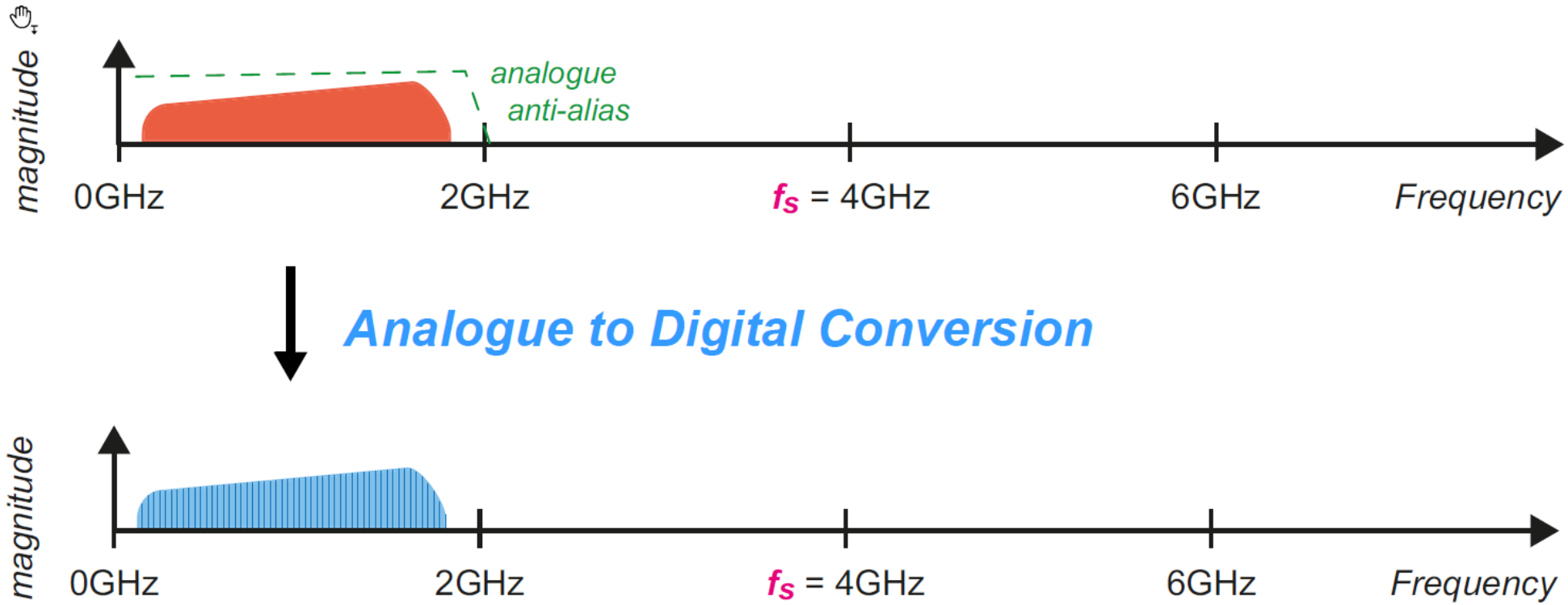
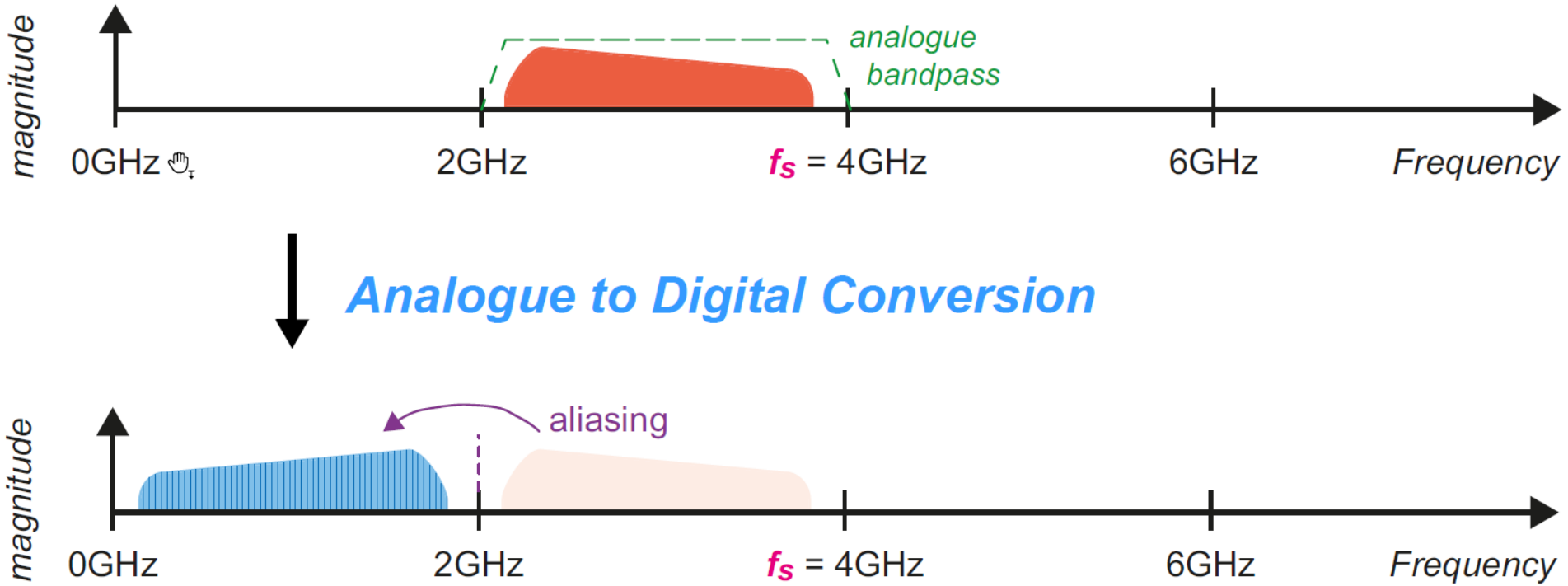
RF ADC and RF DAC in 1st and 2nd Nyquist Zones

- Using 4.096 Gsps/GHz sampling, analogue signals present in the range 0 to 2GHz (i.e. the 1st Nyquist Zone) can be '*traditionally*' digitised in the conventional manner. An analogue anti-alias filter attenuates frequencies above 2GHz.



RF ADC and RF DAC in 1st and 2nd Nyquist Zones

- Signals present in the **2nd Nyquist Zone** can also be captured (by exploiting aliasing (with an appropriate bandpass filter first removes any components present at other frequencies!)



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XUP Edu Notebooks - Wireless Comms / SDR Design

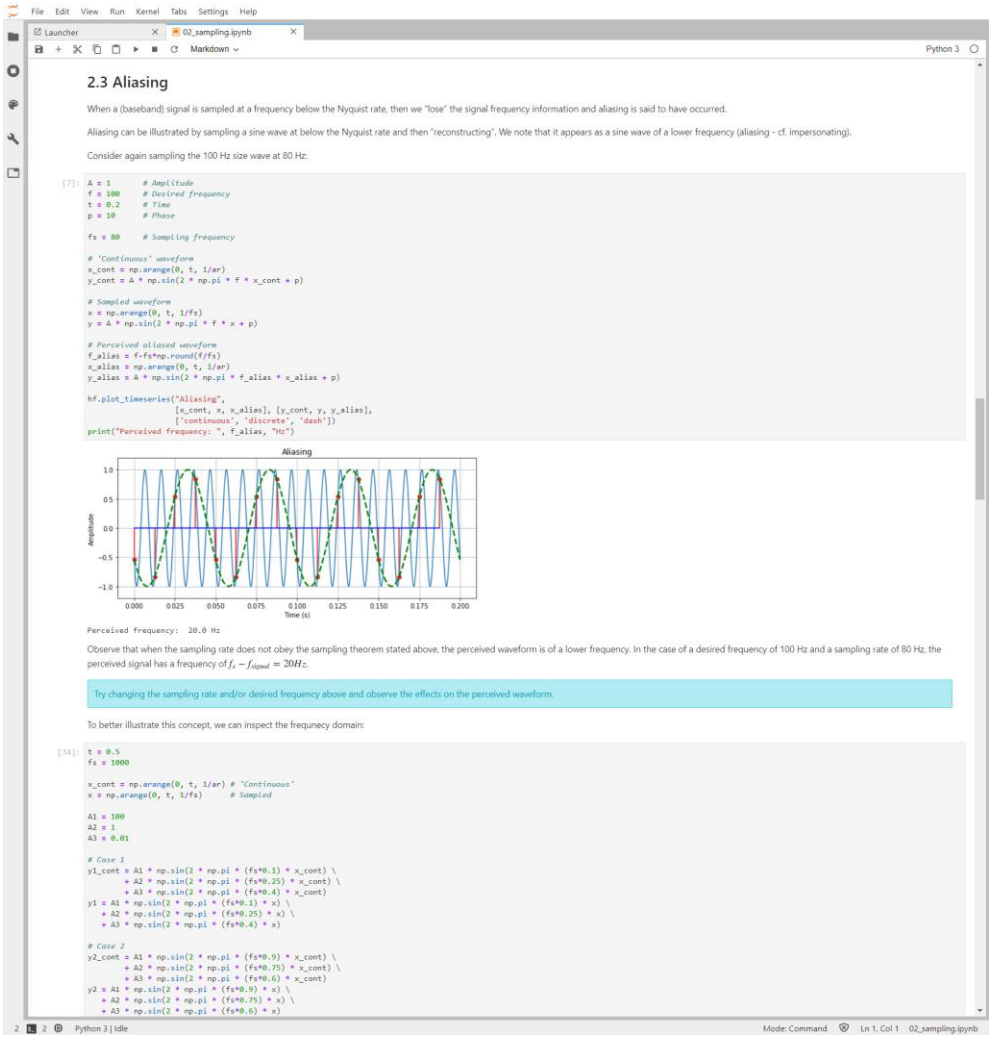
University of Strathclyde

Fundamentals:

- Sampling and Quantisation
- Frequency Spectrum
- Baseband Modulation
- Digital Filters
- Modulation and Demodulation
- RFSoC Architecture Introduction

Advanced:

- OFDM Transmit and Receive (1024 QAM)
- Machine Learning (Modulation Classification)



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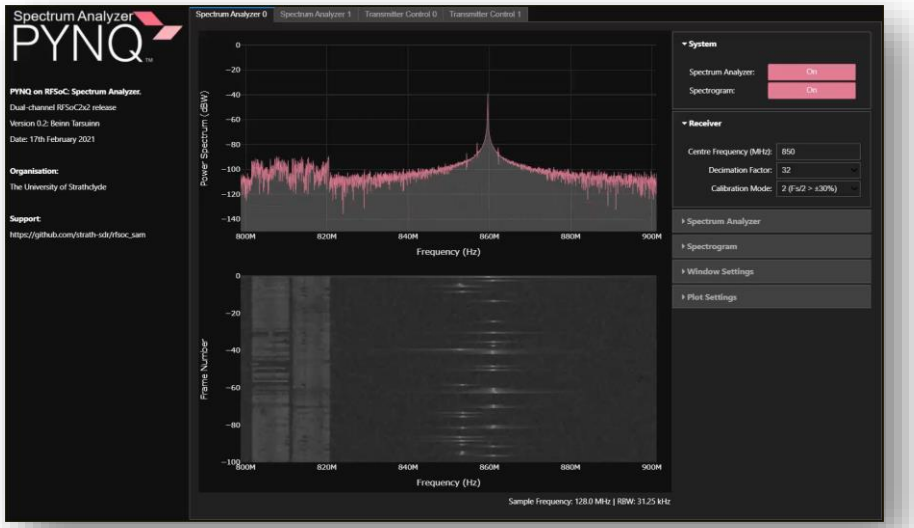
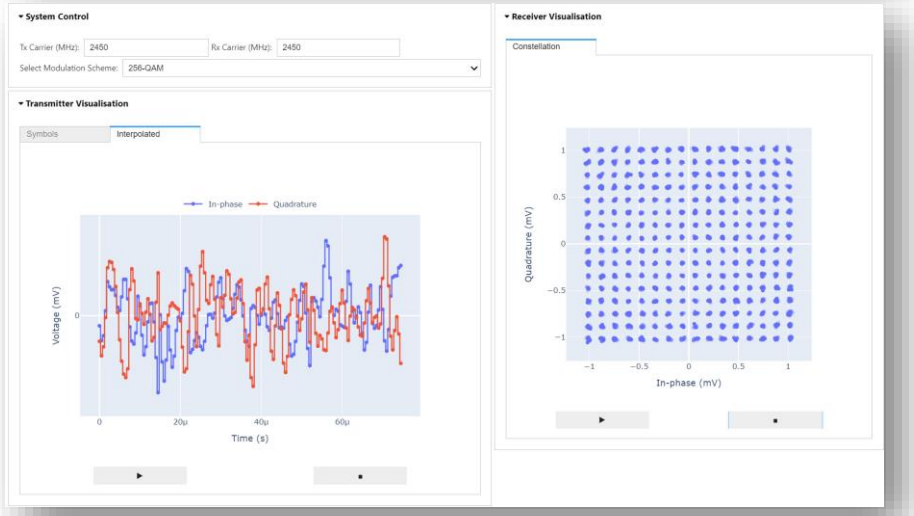
XUP Overlay Demonstrators - Wireless Comms

University of Strathclyde

XUP RFSoC 2x2 includes (Ref Designs):

- Spectrum Analyser
- OFDM RF Transmitter and Receiver
- QPSK RF Transmitter and Receiver
- BPSK RF Transmitter and Receiver
- AGC – Automatic Gain Control Design





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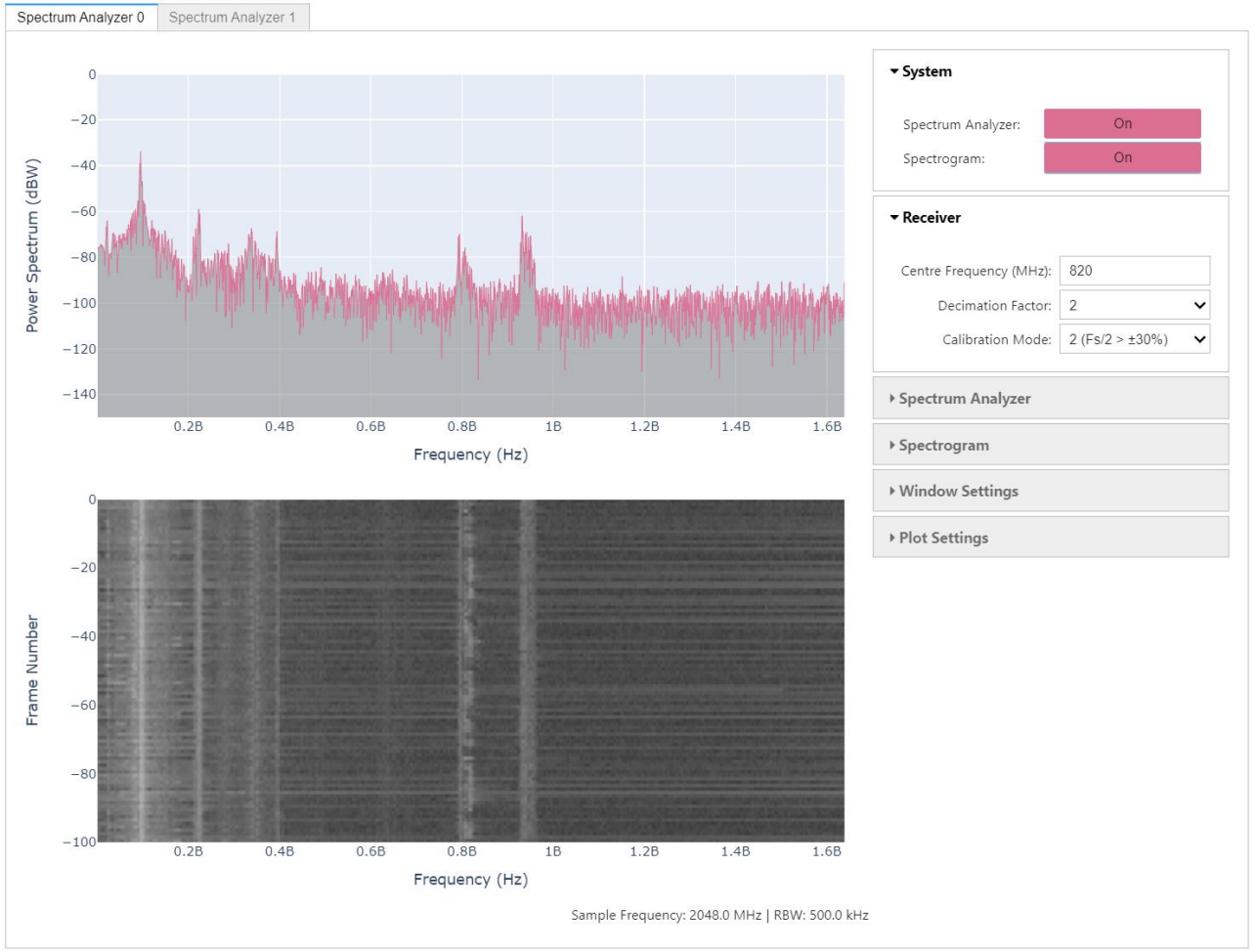
PYNQ Spectrum Analyzer – Ready to Run Instantly!

A Jupyter Dashboard:

- Spectrum Plot
- Spectrogram
- Centre Frequency Selection
- Decimation Control
- Programmable Window
- Dual-Channel (RFSoC2x2)
- Quad-Channel (ZCU111)



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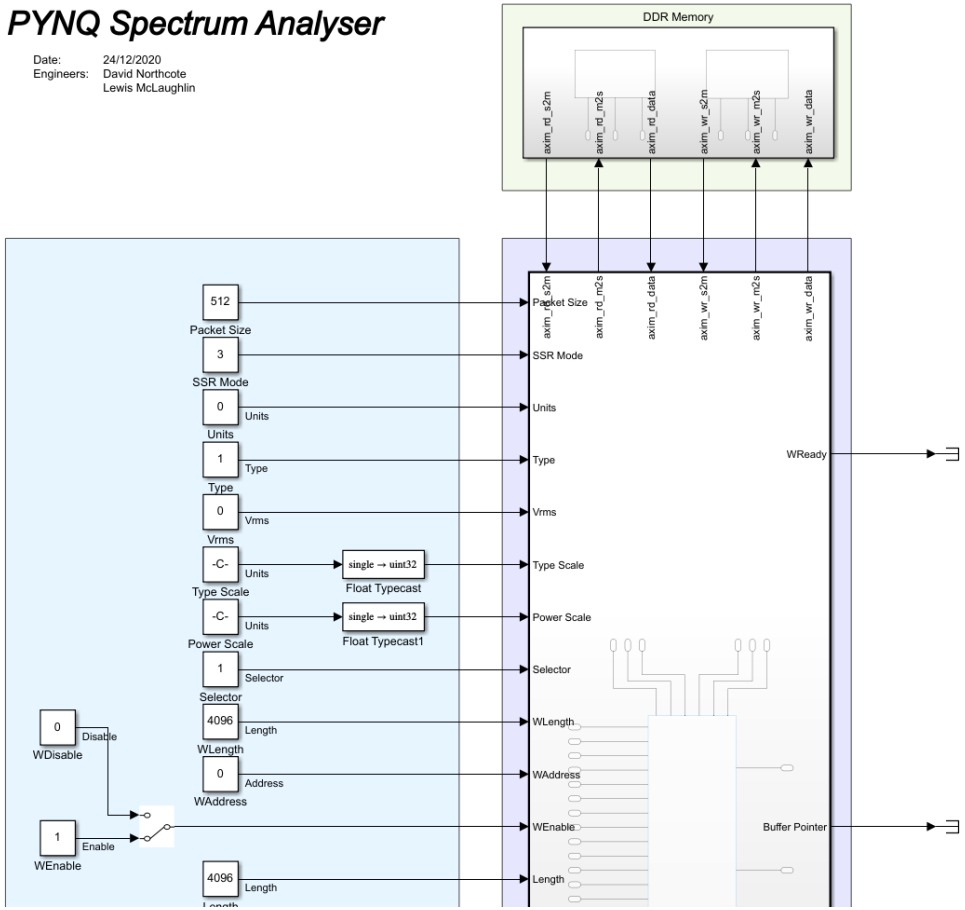
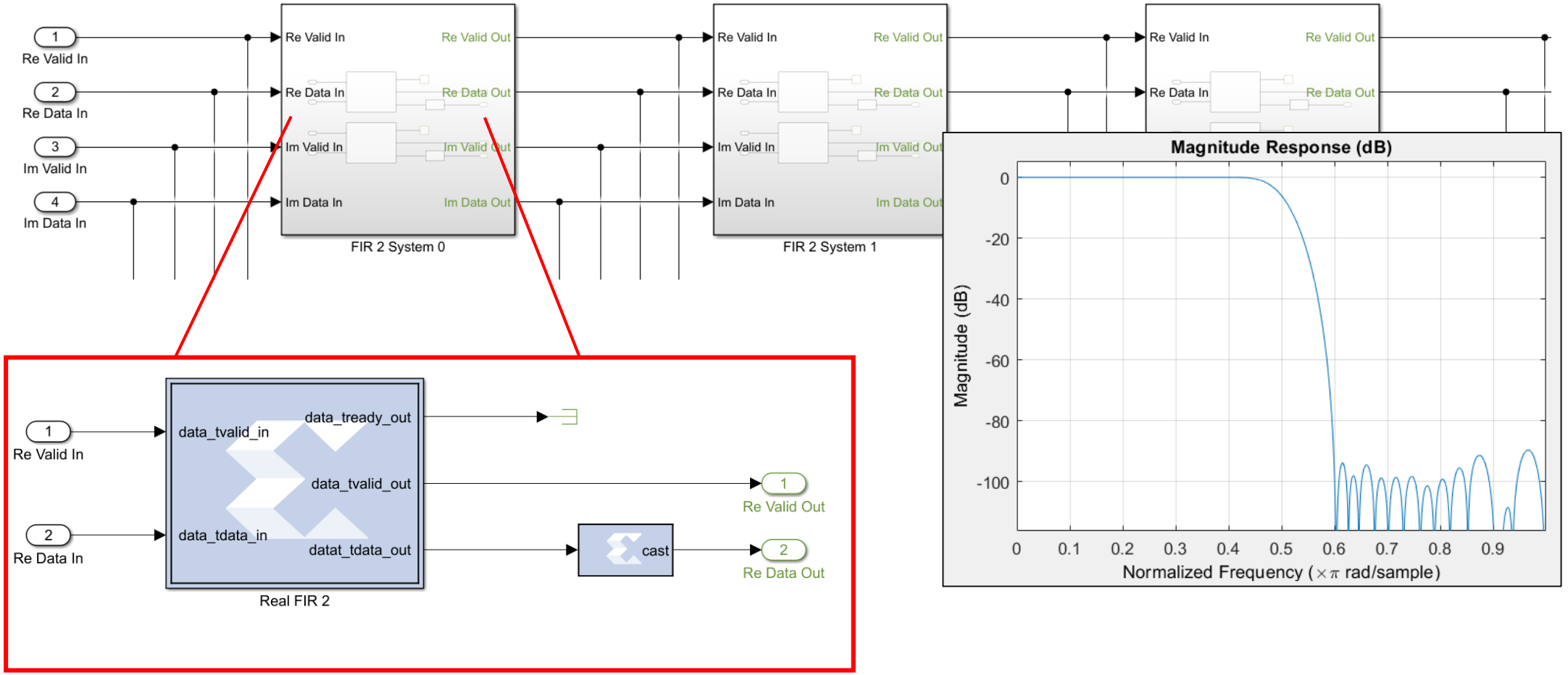
Under the Hood:
DSP Design with Mathworks' *HDL Coder*

- Using Mathworks' HDL Coder in Simulink
  - Enables Model Based Design
  - Large library of prebuilt DSP/HDL blocks
- Using Xilinx System Generator in Simulink
  - Leverage Xilinx IP and Cores
- Easy to integrate into a PYNQ design
  - IP Core Generation
  - Auto Infer AXI Interfaces
- Memory Interface Simulation
  - Supports data transfer modelling with external memory
  - Suitable for FFT frame transfers



SDR Design : A Flexible Decimator in System Generator

A Cascade of Half-Band Filters



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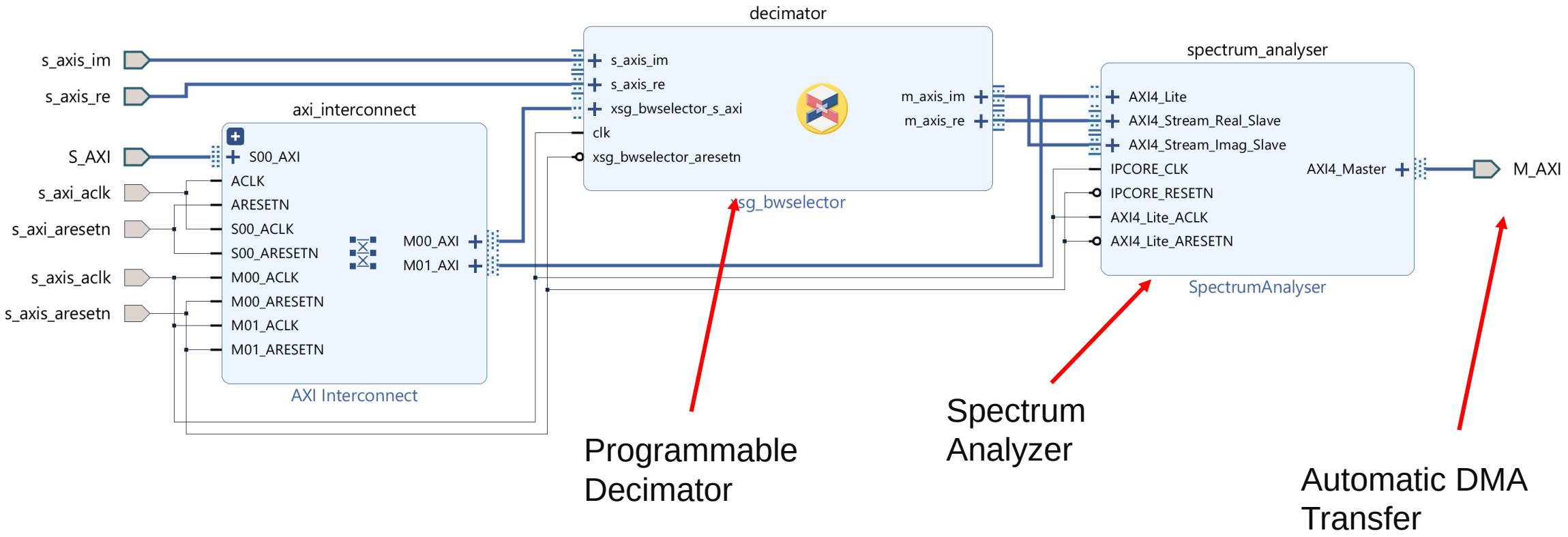
Channel Hierarchy: Spectrum Analyzer



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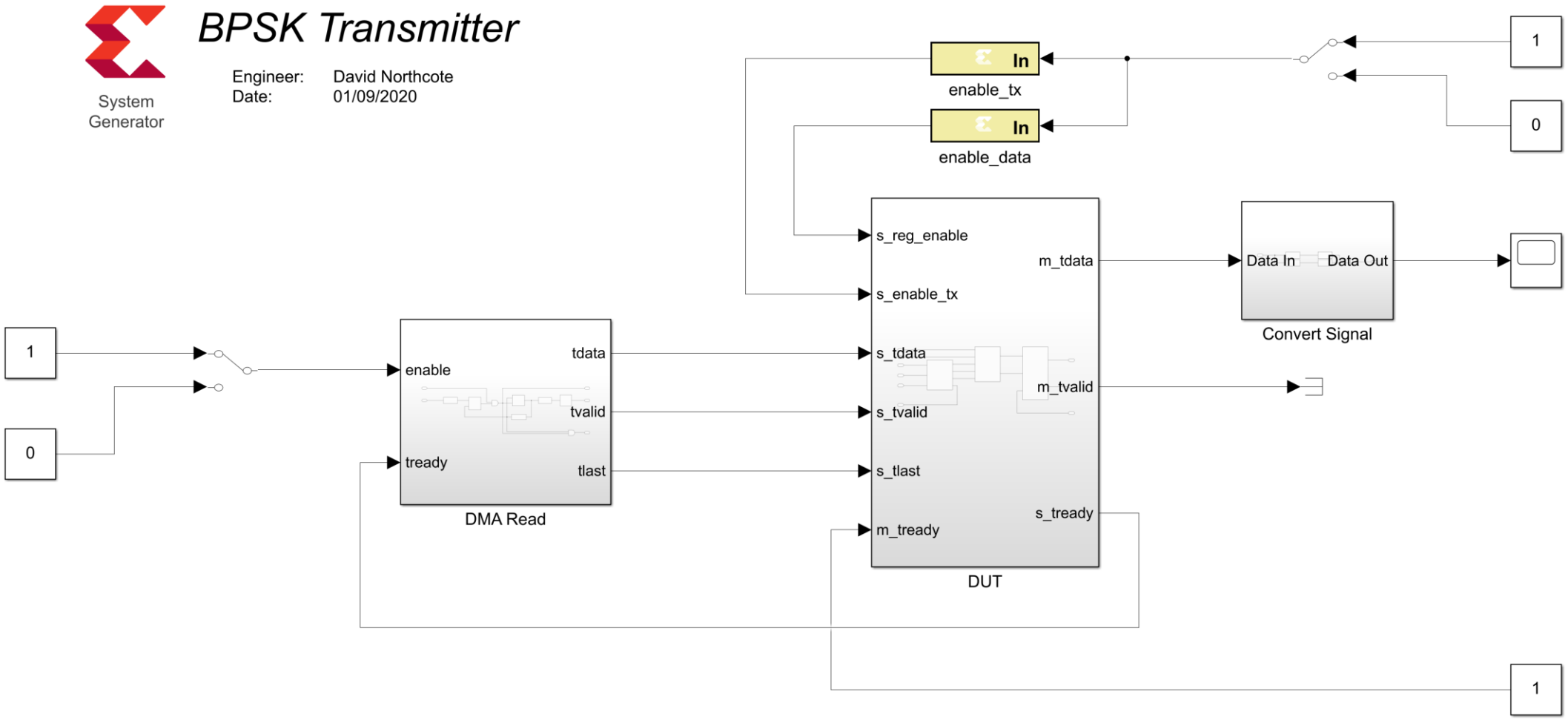
BPSK Transmitter System Generator



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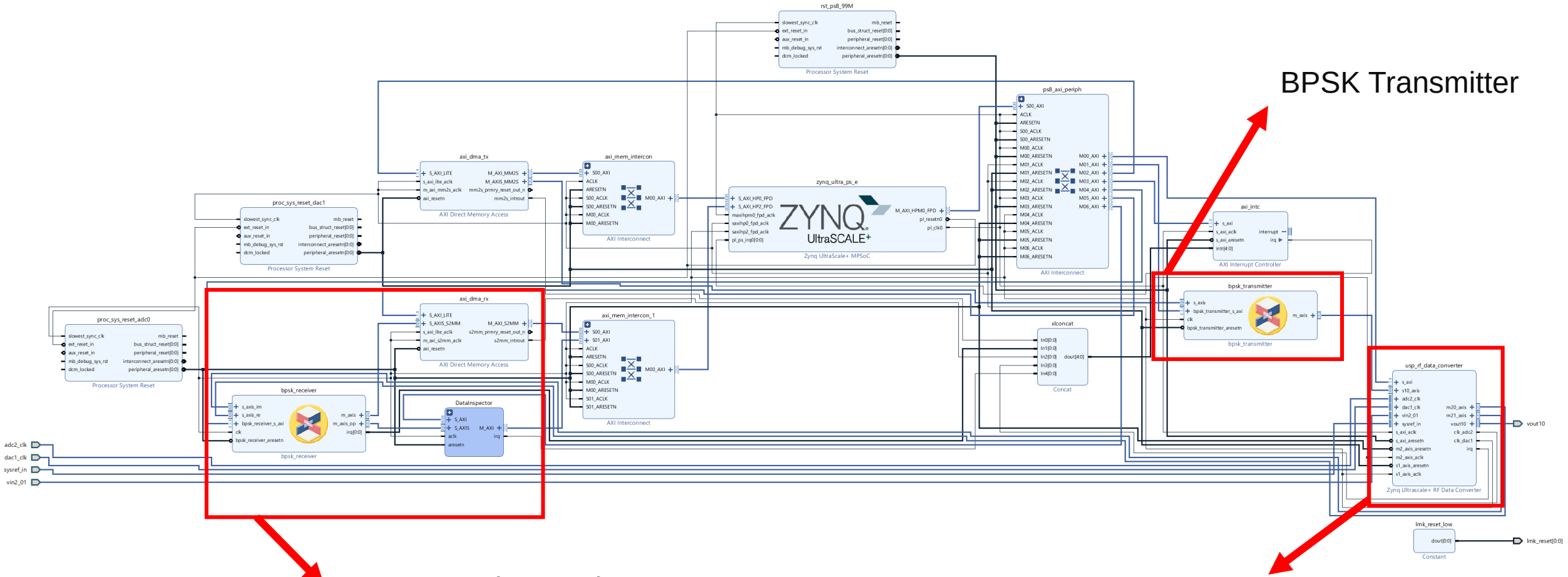
Creating Overlays for RFSoC 2x2



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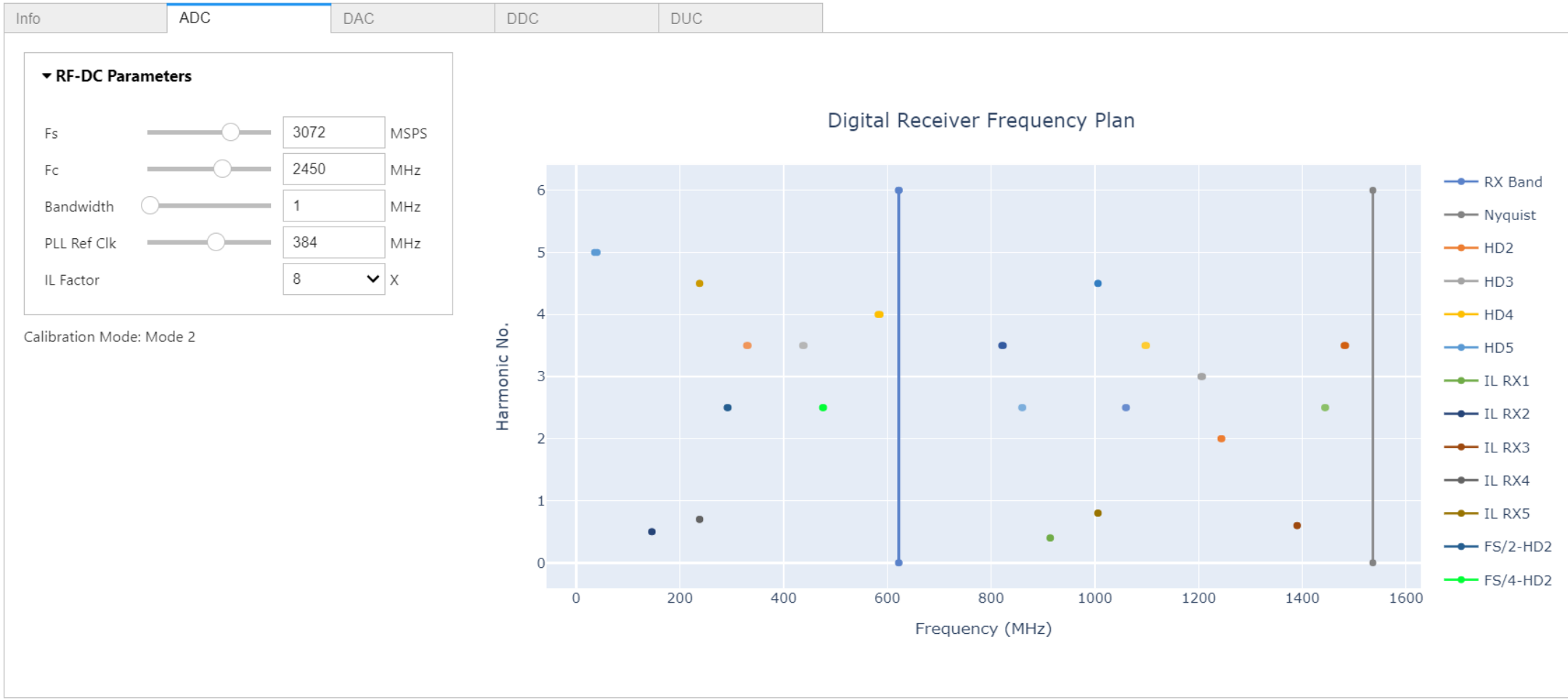
The Receiver Frequency Planner



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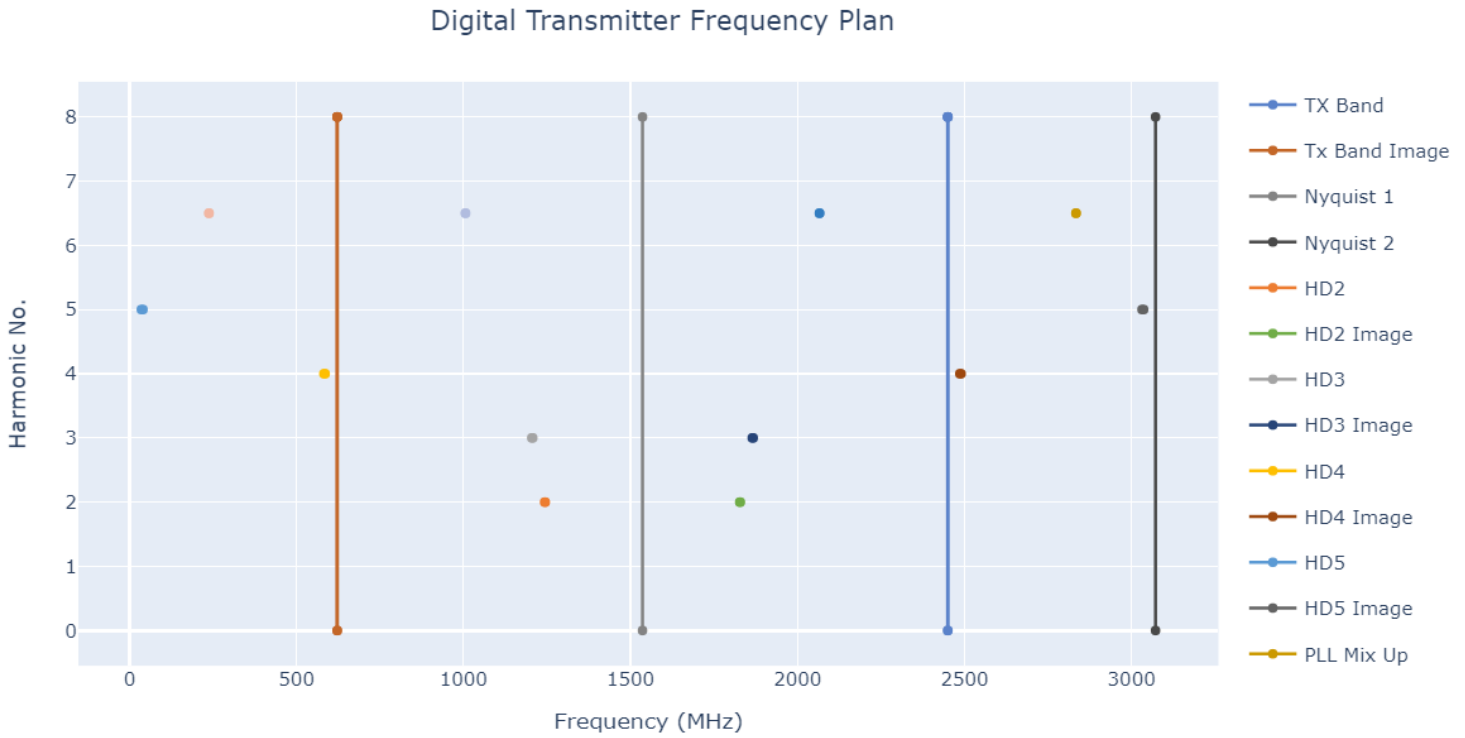
The Transmitter Frequency Planner

Info | ADC | DAC | DDC | DUC

RF-DC Parameters

Fs	3072	MSPS
Fc	2450	MHz
Bandwidth	1	MHz
PLL Ref Clk	384	MHz

Mix Mode: ON



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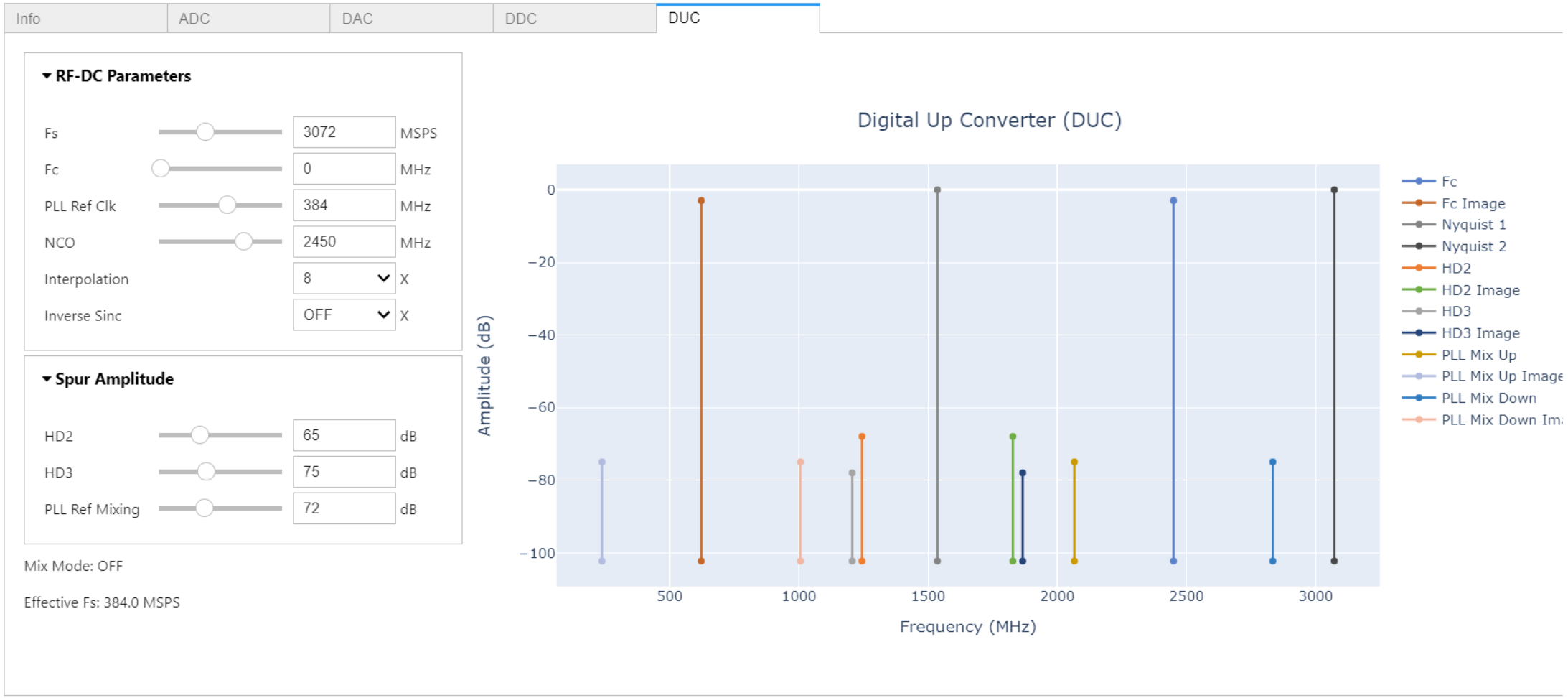
The Digital Up Converter Frequency Planner



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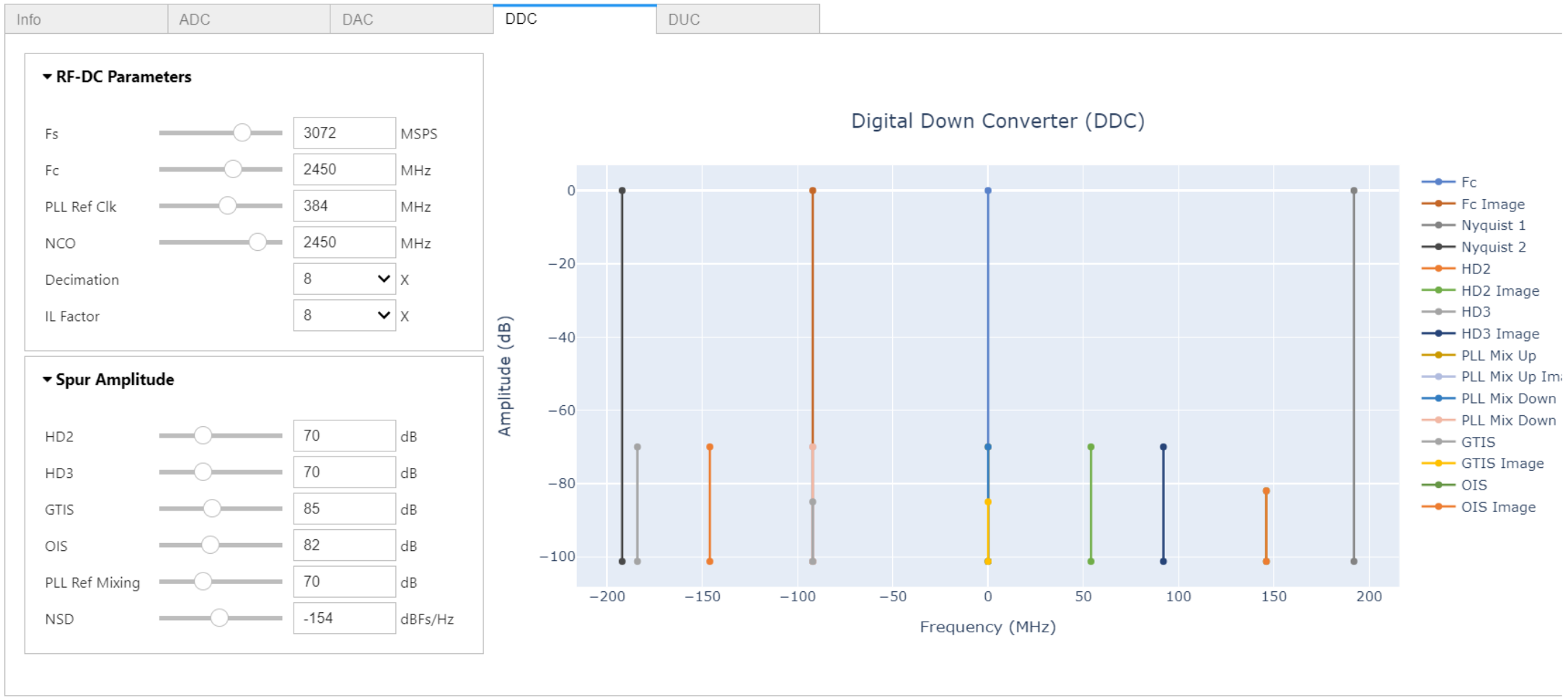
The Digital Down Converter Frequency Planner



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Thank You