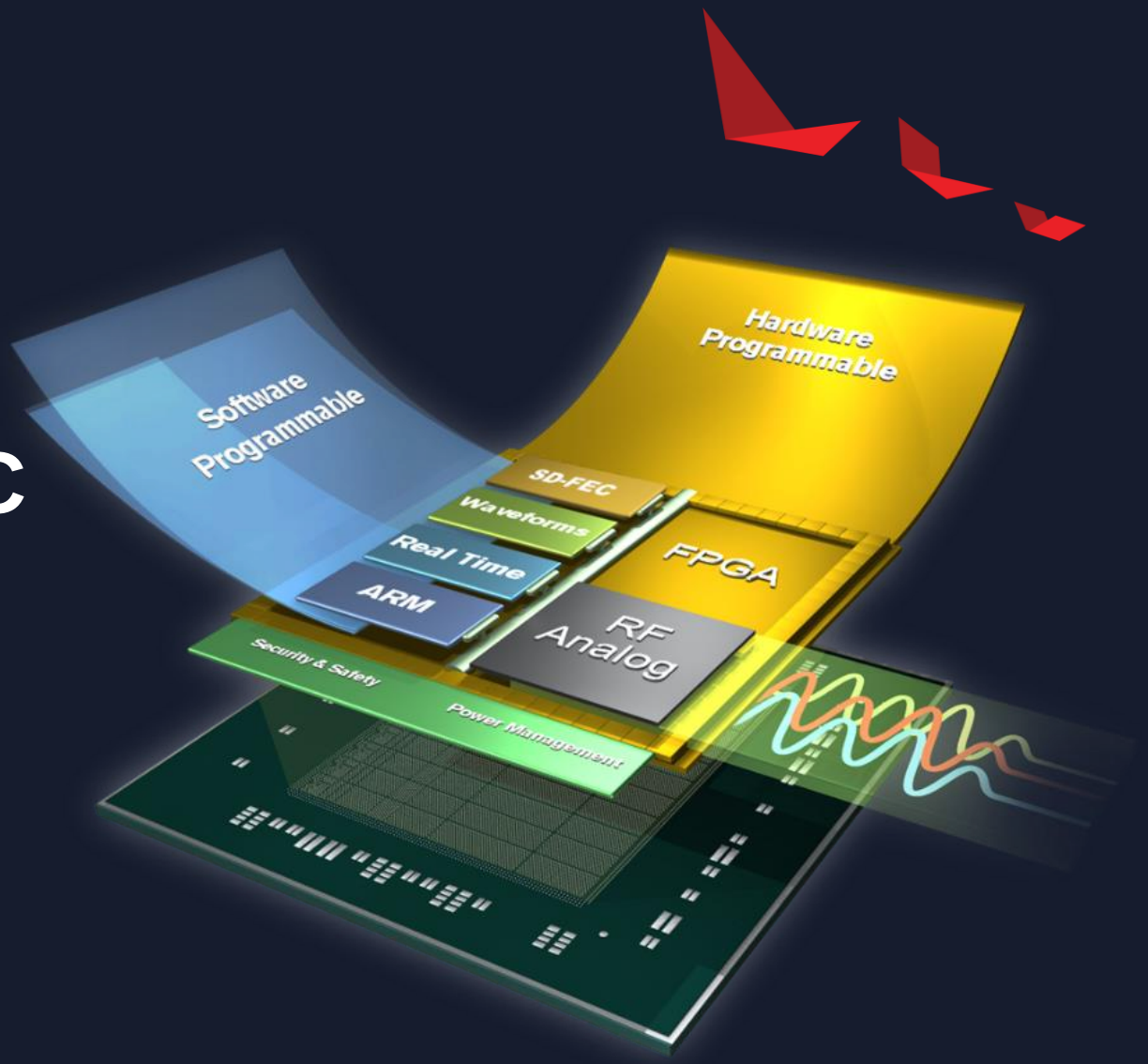
Zynq UltraScale+ RFSoC

The First Hardware Programmable RF System-on-Chip (RFSoC)



- ✓ Zynq UltraScale+ MPSoC
- ✓ Integrated RF-Class Analog
- ✓ Soft-Decision Forward Error Correction (SD-FEC)

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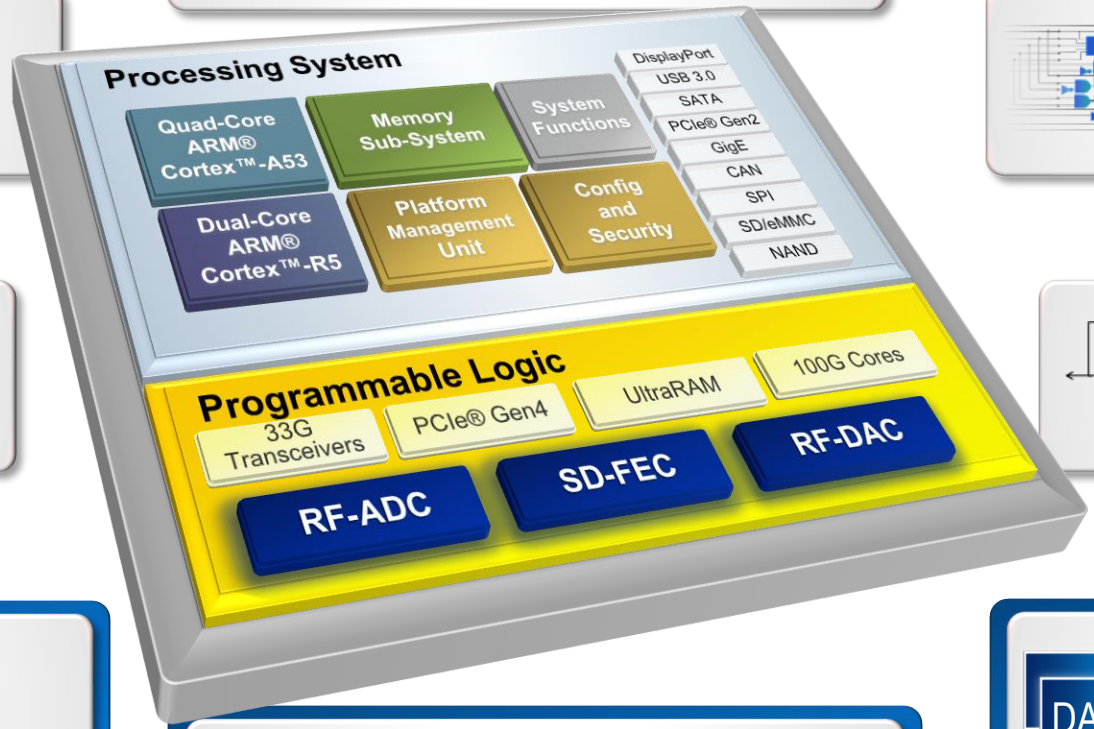
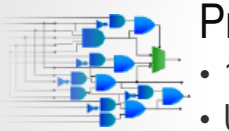
Monolithically Integrated RF-Analog on a Production Proven MPSoC Architecture

Monolithically Integrated

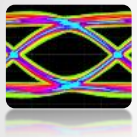
Processing System
- Quad-Core A53 (64-bit)
- Dual-Core R5 (32-bit)

Hardened Engines
- PCIe Gen3 & Gen4
- 100G Cores





Programmable Logic
- 16nm FinFET
- UltraScale+ FPGA Fabric

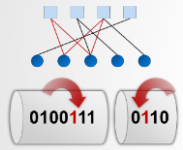


33G Transceivers
- 33Gb/s
- 28G Backplane Capable

DSP-Intensive
- 4,272 DSP slices
- 7,612 GMACs

Integrated Direct-RF Analog-to-Digital Converters

Integrated Direct-RF Digital-to-Analog Converters



Soft Decision Forward Error Correction

LDPC & Turbo Support

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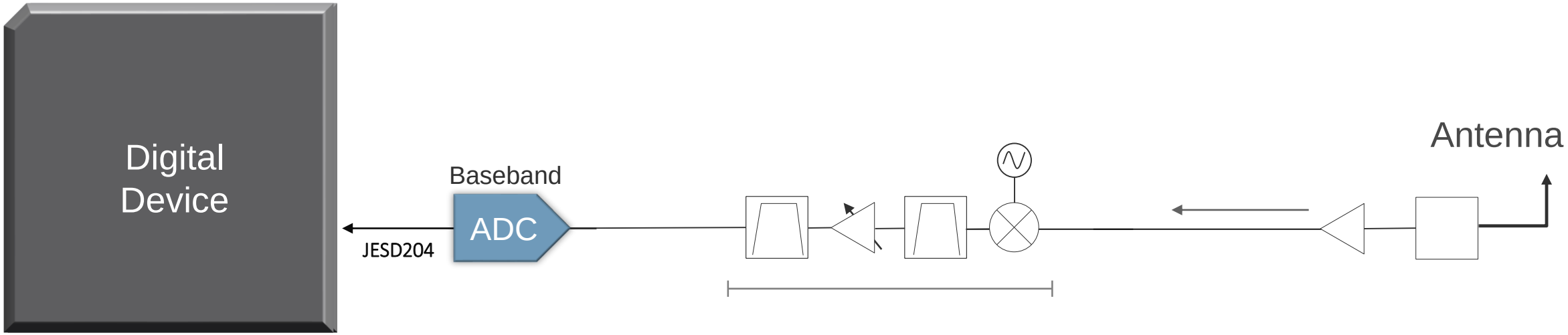
Platform Flexibility with Direct RF-Sampling

Traditional **IF** (*Intermediate Frequency*) **Sampling**

Signal conditioning **before** ADC sampling using **analog** components



Analog-Based Signal Conditioning

- ✓ Power efficient
- ✗ Greater footprint due to multiple components
- ✗ Greater design effort due to BOM complexity
- ✗ Limited flexibility due to fixed components

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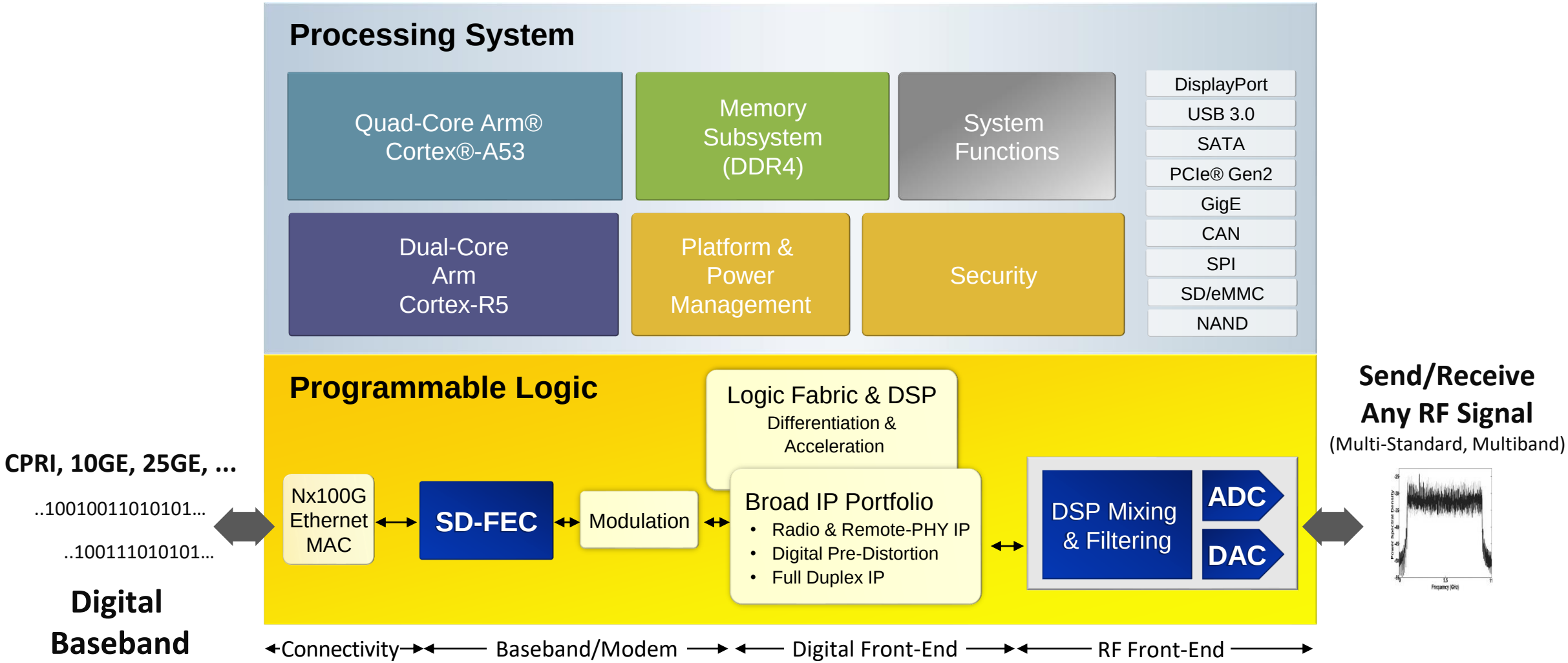
Single Chip Adaptable Radio Platform



Integrating the RF Signal Chain

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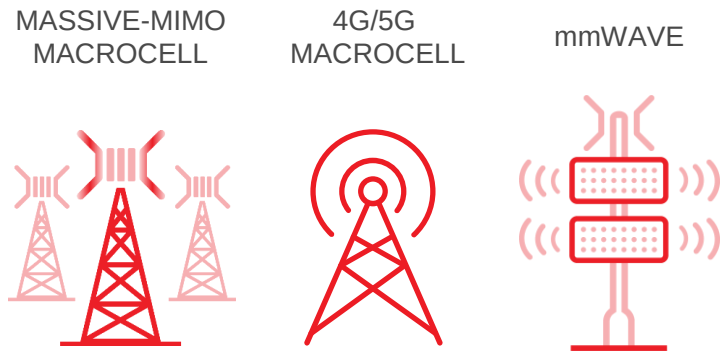
Key Target Markets and a Breadth of RF-Applications

WIRELESS

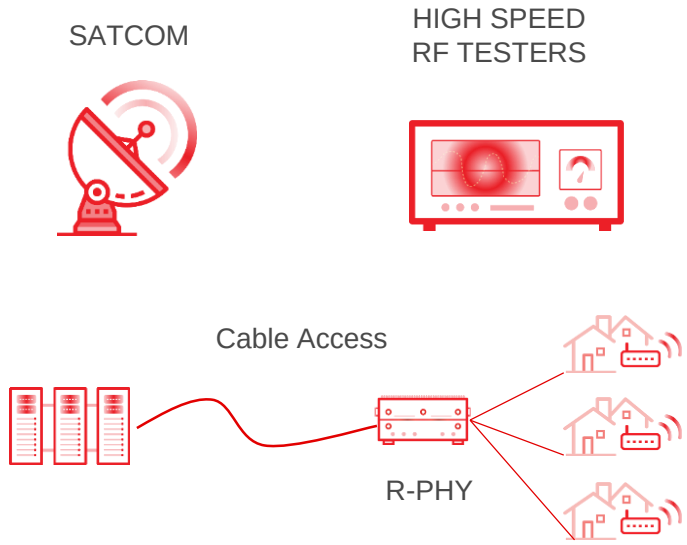


- Power & Footprint for mMIMO
- Multi-band, multi-mode for Macro
- IF Digital Transceiver for mmWave 5G NR

AEROSPACE & DEFENSE

- SW & HW Reconfigurable
- Full L-Band & S-Band Sampling
- Partial C-Band Direct Sampling

BREADTH OF RF APPLICATIONS



- Test & Measurement
- Satellite Communications
- Cable Access

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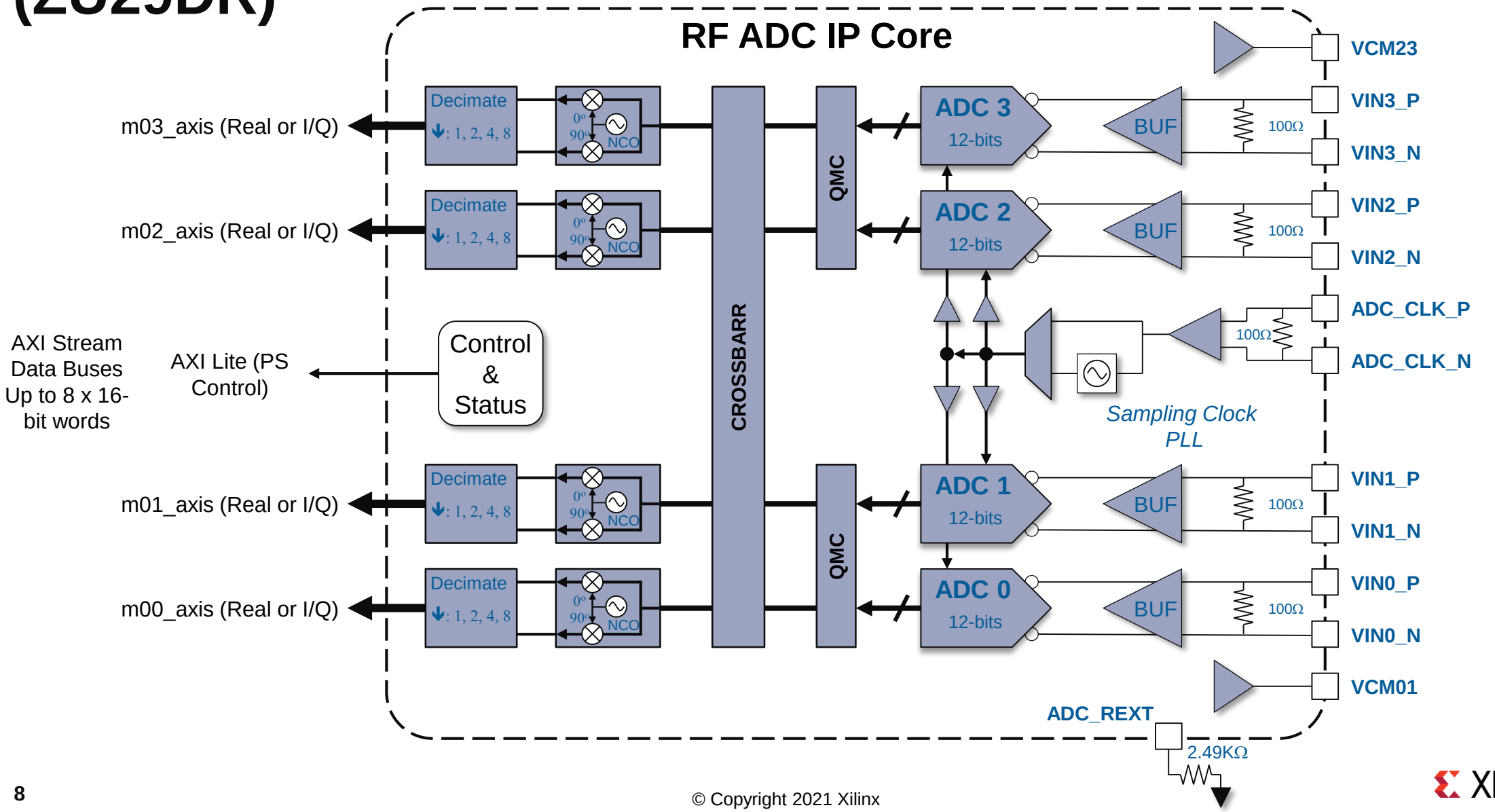
RF Data Converter IP Blocks

RF ADC GEN 1 Block Quad ADC Tile Configuration (ZU29DR)



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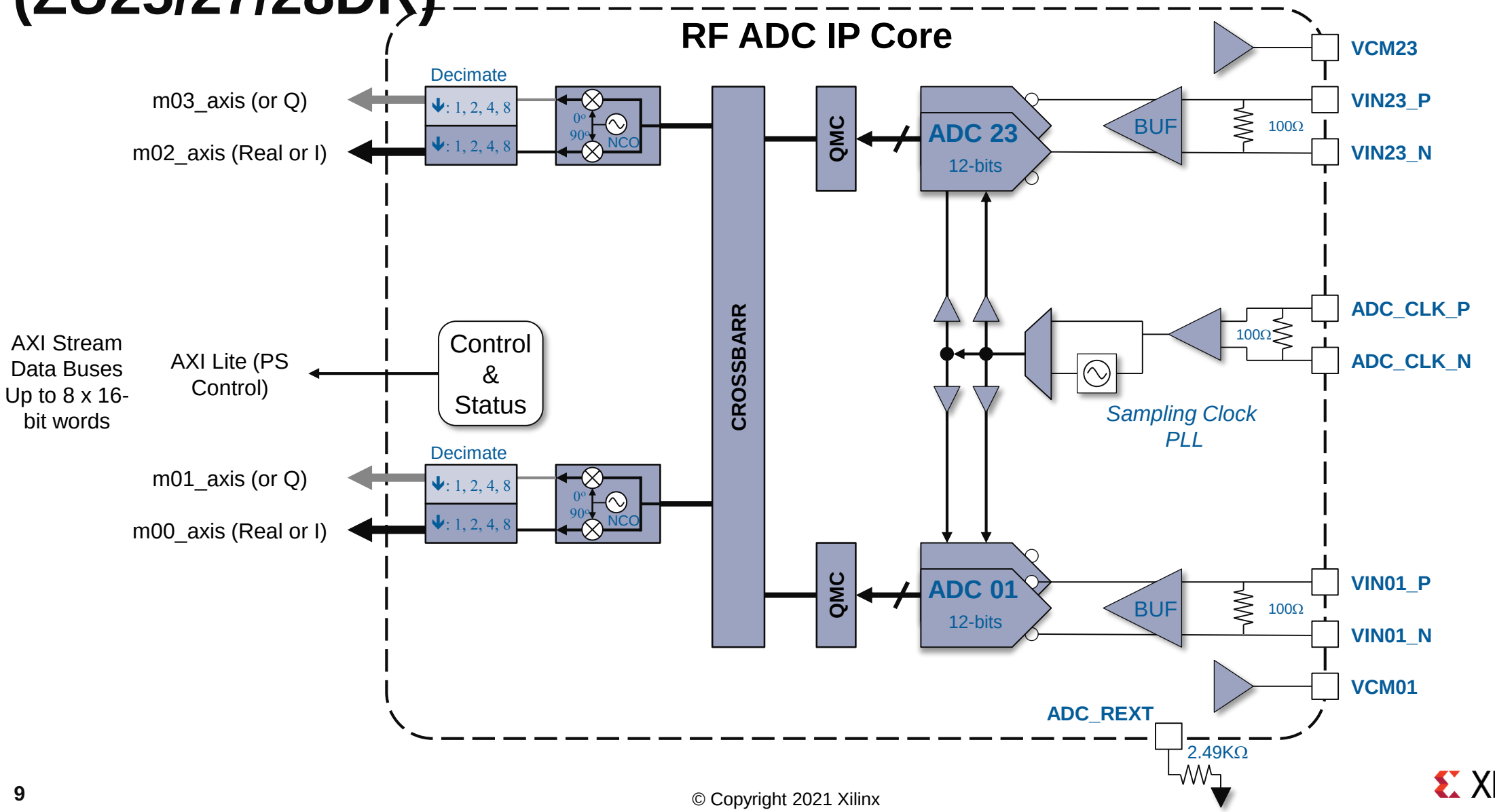
RF ADC GEN 1 Block Dual Tile ADC Configuration (ZU25/27/28DR)



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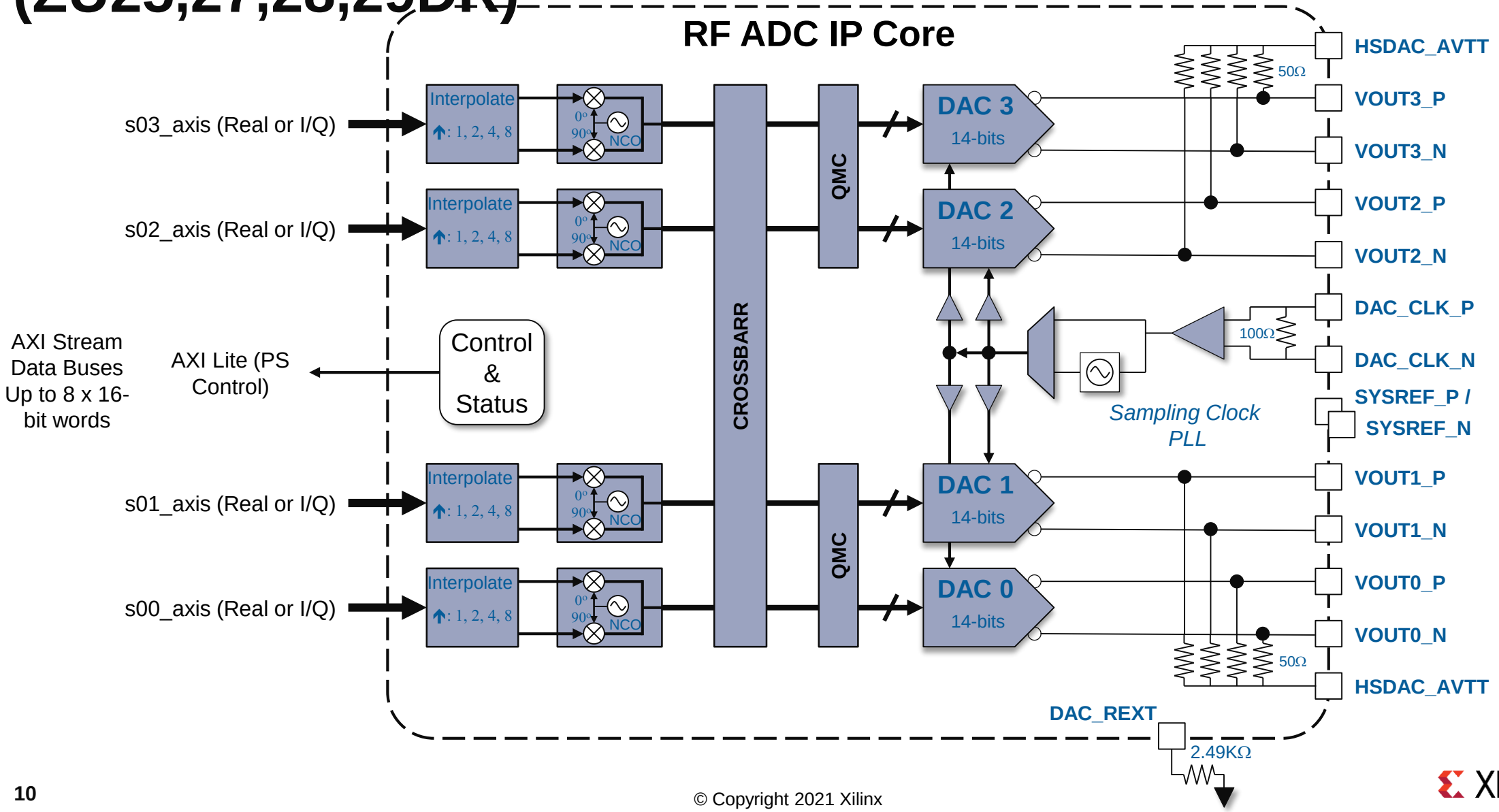
RF DAC GEN 1 Block Quad DAC Tile Configuration (ZU25,27,28,29DR)



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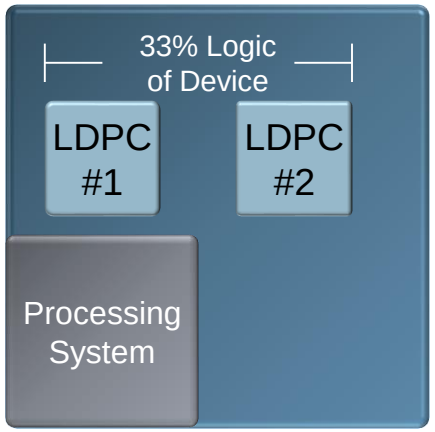
Soft-Decision Forward-Error-Correction (SD-FEC)
Hard IP vs Soft IP

- 307MHz F_{MAX}
- 150k LUTs
- 258 BRAM Kbits for storage & buffering

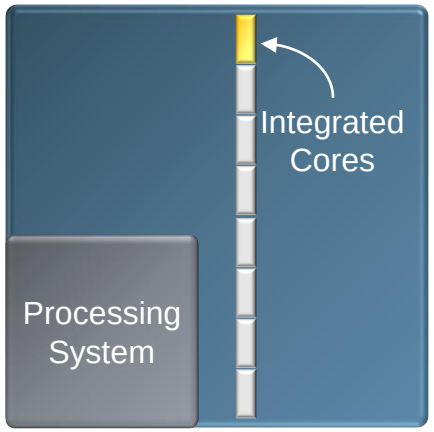
LDPC FEC Soft Cores
~1M System Logic Cells (425K LUTs)



~6.4W of Dynamic Power

80%
Power Reduction

Integrated SD-FEC
(ZU21DR RFSoC)



~1.2W of Dynamic Power

- 614MHz F_{MAX}
- No additional resources required
- More flexibility & functionality available vs. soft core
- 8X user configurable SD-FEC blocks
- 19.8Gb/s LDPC encode throughput
- 2.84Gb/s @8 iterations LDPC decode throughput
- 1.78Gb/s @6 iterations turbo decode throughput

- SD-FEC LDPC codec meets specifications of 5G and DOCSIS 3.1
- Custom code construction to evolve with standards
- Turbo decode for 4G LTE-Advanced and 4G LTE-Pro compliance

Zynq UltraScale+ RFSoC Gen 1 Product Table

		ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR
Analog-Digital Signal Chain	12-bit, 4.096 GSPS ADC	-	8	8	8	–
	12-bit, 2.058 GSPS ADC	–	–	–	-	16
	14-bit, 6.554GSPS DAC	-	8	8	8	16
	SD-FEC	8	–	-	8	–
Processing System & Programmable Logic	Application Processor Core	Quad-core ARM Cortex-A53 MPCore up to 1.33GHz				
	Real-Time Processor Core	Dual-core ARM Cortex-R5 MPCore up to 533MHz				
	High Speed Connectivity	DDR4-2666, PCIe Gen3 x16, 100G Ethernet				
	Logic Density (System Logic Cells)	930K	678K	930K	930K	930K
	DSP Slices	4,272	3,145	4,272	4,272	4,272
	33G Transceivers (Max)	16	8	16	16	16
Packages	35mmx35mm	D1156	E1156	E1156	E1156	
	40mmx40mm		G1517	G1517	G1517	
	42.5mmx42.5mm					F1760

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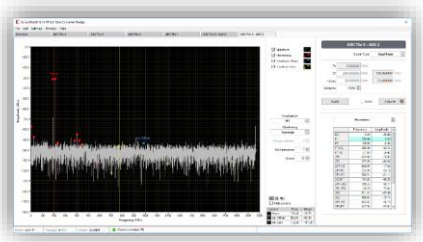
Zynq UltraScale+ RFSoC Gen 1 in Production

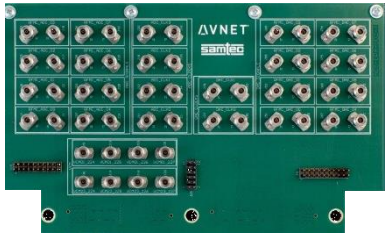
- **All Devices in Production**
  - Lidded and Lidless all Available
  - Vivado & SDK, documented flows

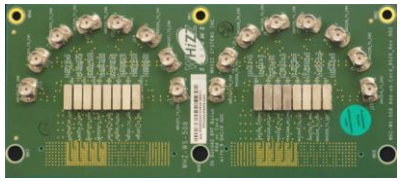
- **ZCU111 Evaluation Kit – Shipping Now**
  - 8x8 Evaluation board equipped with ZU28DR Production Silicon
  - Includes cables, filters and XM500 Balun Transformer Card

- **RF Eval Tool: Targeted Reference Design Available now–**
  - Evaluate RF Capabilities through Ethernet for ZCU111
  - Multiband configuration management
  - User friendly GUI



- Available daughter cards
  - Differential break-out card from Avnet
  - Band 42 Balun daughter card available from partner Whizz Systems





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ZU28DR SFDR at FS=3.93216GS/S, Fin=240MHz@-1dBFS

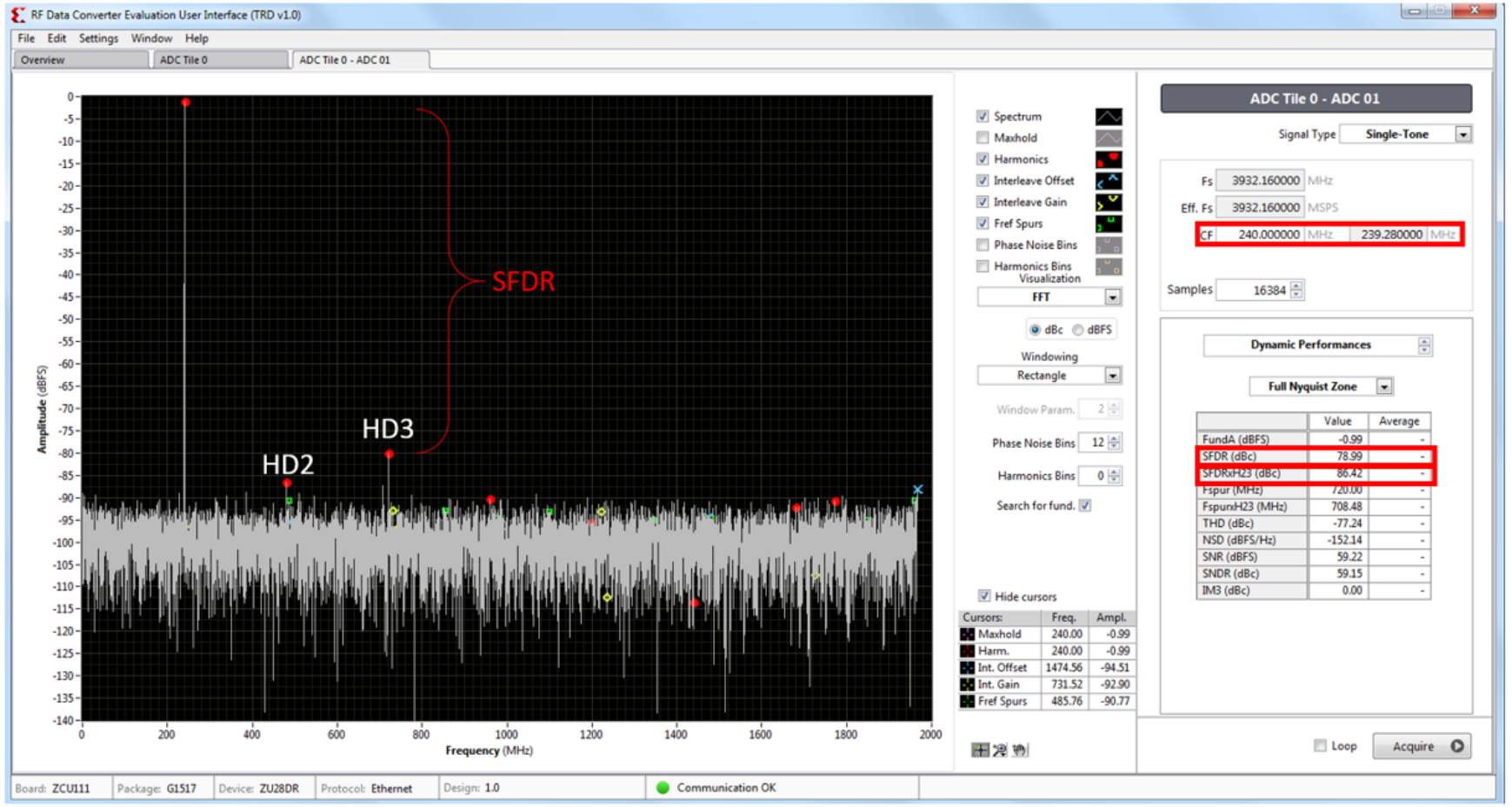

Figure 1: Xilinx UltraScale+ RFSoC 12-bit, ADC Fin = -1dBFS @ 240MHz, fs = 3.93216GSPS, SFDR measured from Xilinx RF Data Converter Evaluation Tool

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ZU28DR ADC NSD at FS=3.93216GS/S, Fin=900MHz

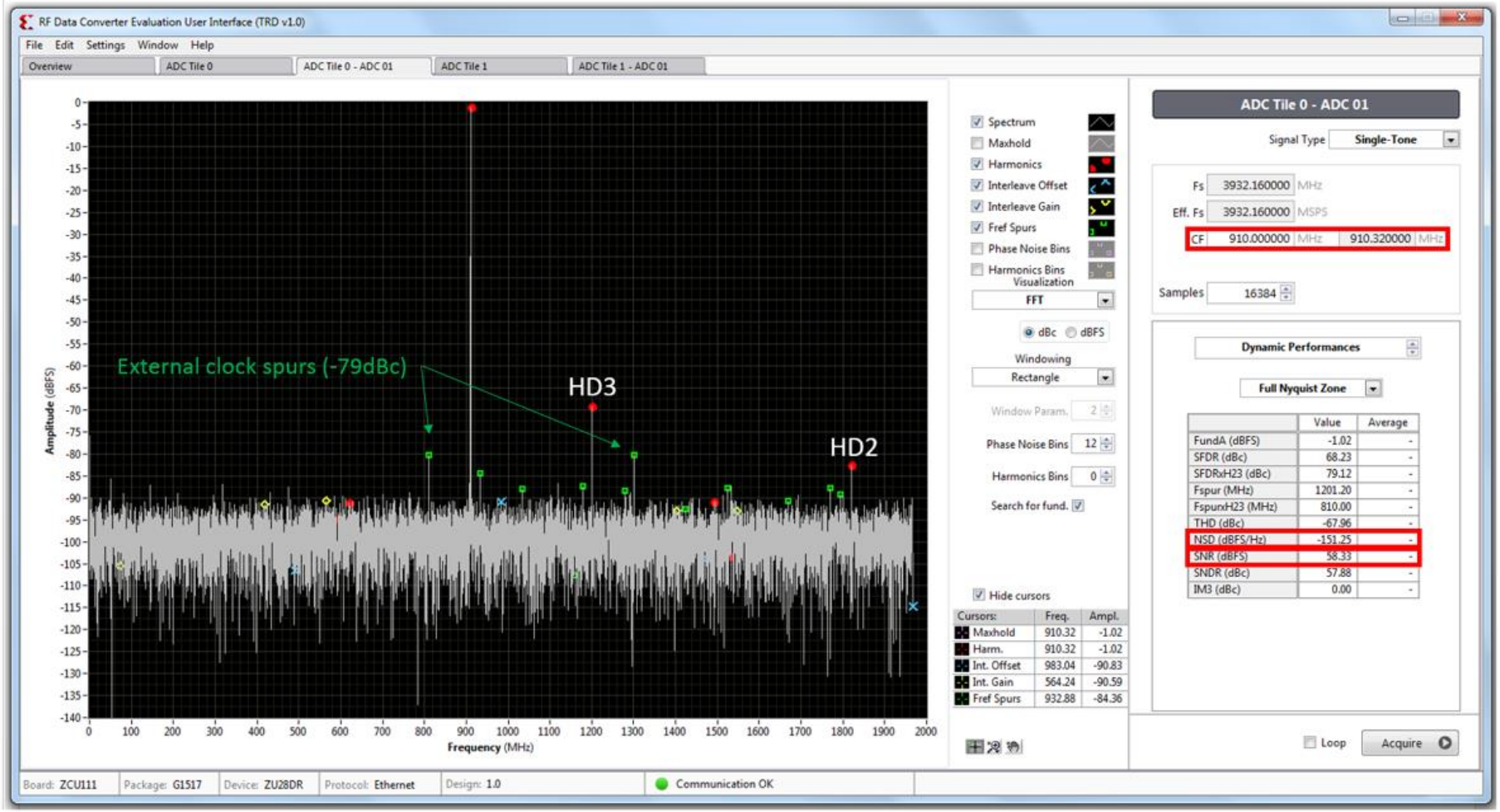

Figure 9: NSD measurement of UltraScale+ RF-ADC on the RF Data Converter Evaluation Tool at 900MHz

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ZU28DR DAC IMD at, Fout=900MHz @-7dBm Pout

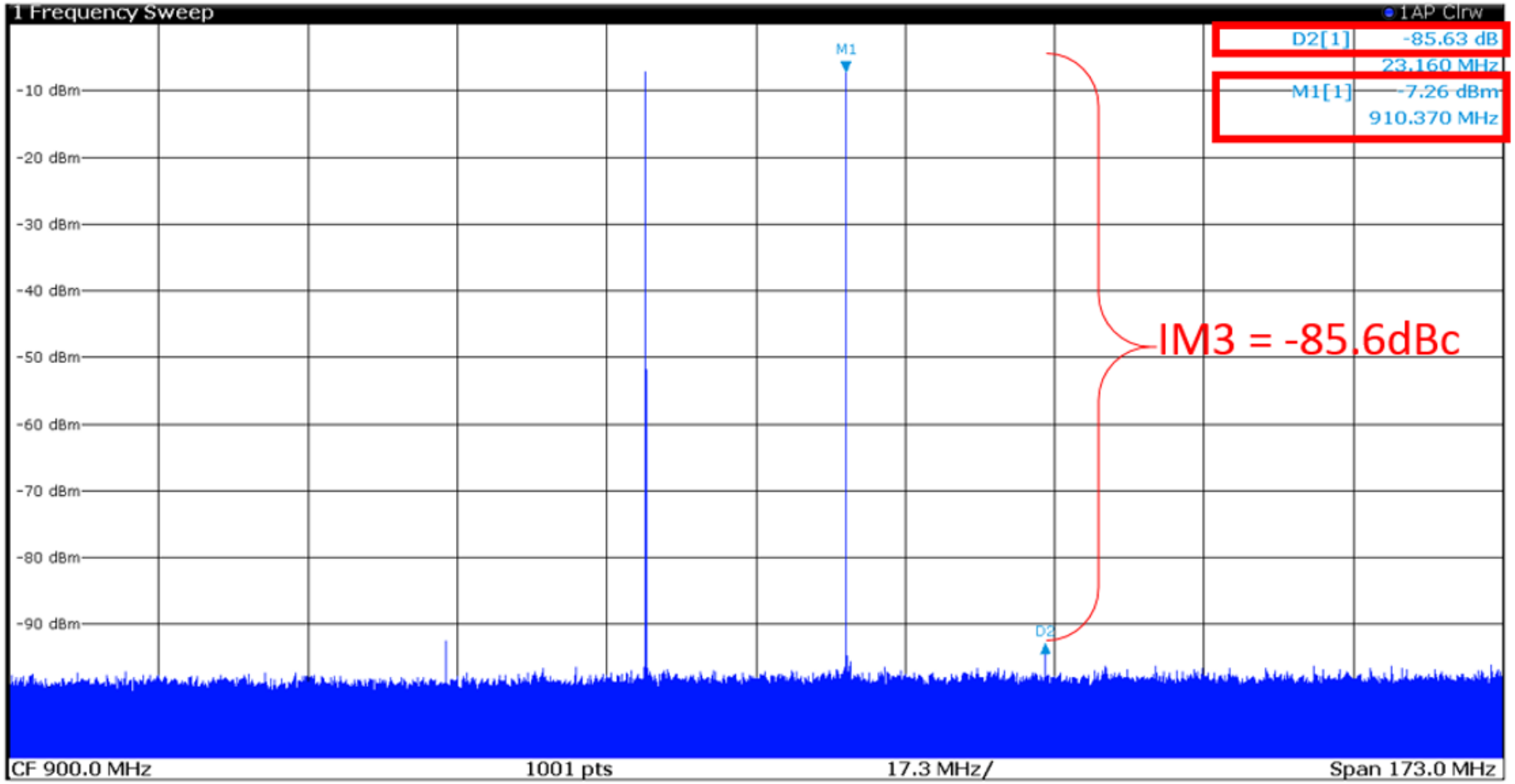

Figure 11: UltraScale+ RF-DAC IM3 measurement with Dual-Tone input

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Roadmap to Meet Current and Future Market Needs

Performance

ZYNQ RFSoC

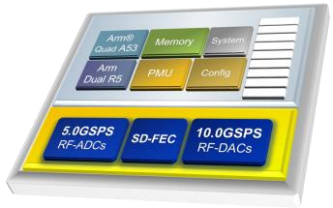
GEN 1

4GHz
of Analog Bandwidth

GEN 2

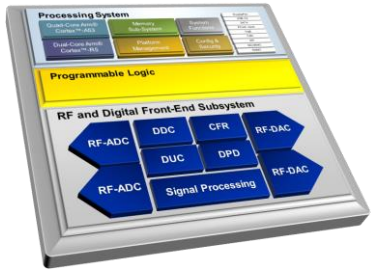
5GHz
of Analog Bandwidth

GEN 3



6GHz
of Analog Bandwidth
8x OR 16x 10.0GSPS DACs
8x 5.0GSPS OR 16x 2.5GSPS ADCs

Zynq RFSoC DFE



7.125GHz
of Analog Bandwidth
With Hard IP Blocks
8x or 6x 10.0GSPS DACs
8x 2.95GSPS & 2x 5.9 GSPS ADCs
or 6x 5.9GSPS ADCs

For more info: www.Xilinx.com/rfsoc

2018 2019 2020 2021 2022

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Scalability Across the Portfolio

				ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR
			Radio		●	●	●	●	●	●		●	●	●	●
			Backhaul				●							●	
			Baseband	●											
			Fixed Wireless Access				●	●	●	●			●		●
			Cable R-PHY				●							●	
			Satellite / Test & Measurement			●		●		●	●		●		●
			Radar / SIGINT					●		●	●	●			●
Analog Signal Chain	RF Data Converter Subsystem	RF-ADC w/DDC	# of ADCs	-	8	8	8	16	16	8 / 2	4	8 / 4	8	8	16
			Max ADC rate (GSPS)	-	4.096	4.096	4.096	2.058	2.220	2.5 / 5.0	5.0	2.5 / 5.0	5.0	5.0	2.5
			Resolution (bits)	-	12	12	12	12	12	14	14	14 / 14	14	14	14
		RF-DAC w/DUC	# of DACs	-	8	8	8	16	16	8	4	12	8	8	16
			Max DAC Rate (GSPS)	-	6.554	6.554	6.554	6.554	6.554	10.0	10.0	10.0	10.0	10.0	10.0
			Resolution (bits)	-	14	14	14	14	14	14	14	14	14	14	14
			SD-FEC	8	-	-	8	-	-	-	-	8	-	8	-
			Real Multi-band support per ADC	-	1	1	1	1	1	1	2	1	1	1	1
			RF input Freq max. GHz	4					5	6					
			Decimation / Interpolation	1x, 2x, 4x, 8x					1x, 2x, 4x, 8x	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x					
Programmable Logic (PL)	Integrated IP		System Logic Cells (K)	930	678	930	930	930	930	488	930	930	930	930	930
			DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	1872	4,272	4,272	4,272	4,272	4,272
			GTY Transceivers	16	8	16	16	16	16	8	16	16	16	16	16
			PCIe® Gen 3x16, * and Gen 4x8	2	1	2	2	2	2	-	2*	2*	2*	2*	2*
			100G Ethernet w/RS-FEC	2	1	2	2	2	2	1	2	2	2	2	2
Package Footprint	D1156	35x35		■											
	E1156	35x35			■	■	■			■	■		■	■	
	G1517	40x40			■	■	■				■		■	■	
	F1760	42.5x42.5						■	■						■
	H1760	42.5x42.5										■			

Package Migration

Package Compatible

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Thank You